Silicon Friendly Materials and Device Solutions for Microenergy Applications

SiNERGY

sinergy-project.eu

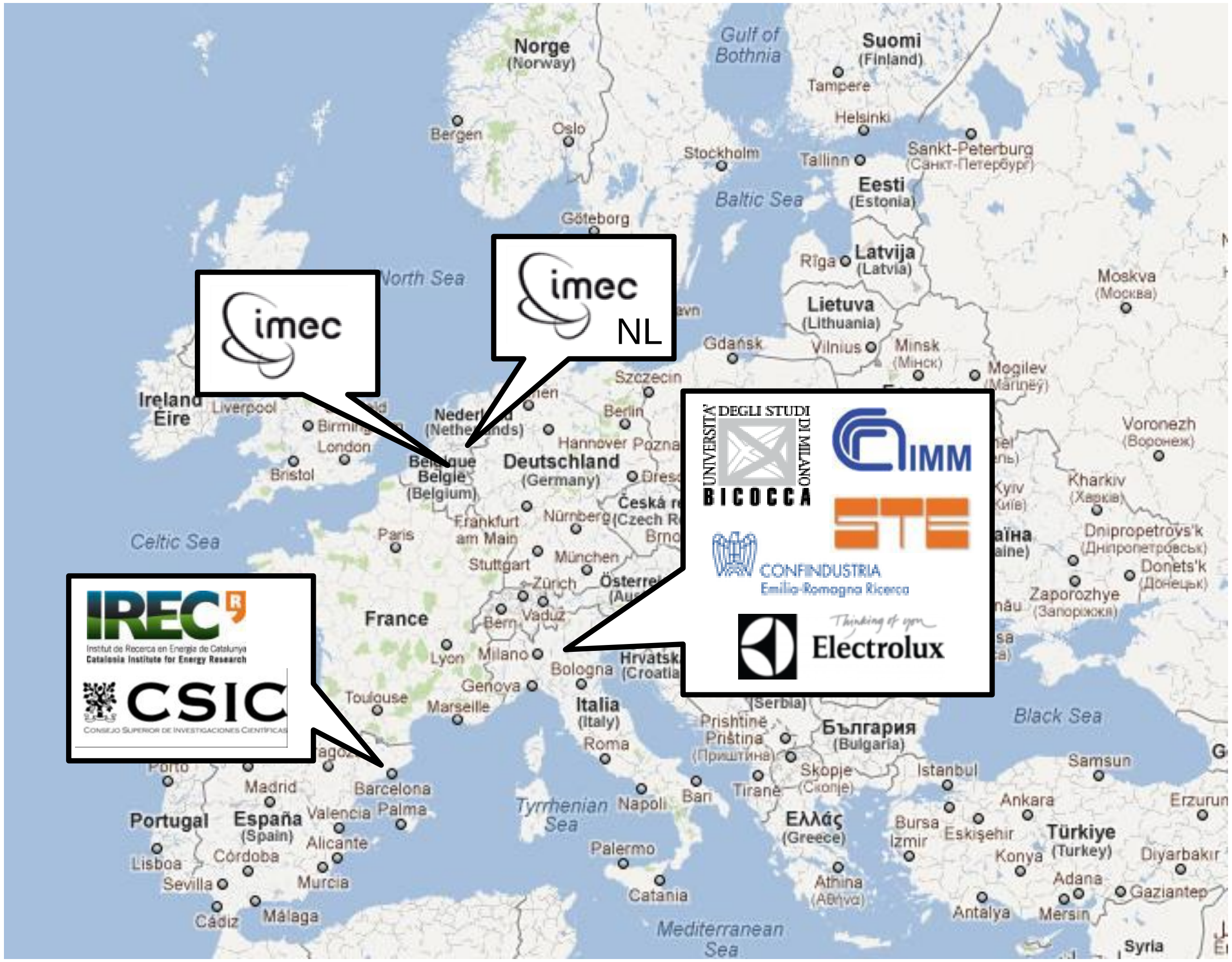
Silicon as a Key Material for Multiphysics Microharvesting: the SiNERGY Project

Dario Narducci,
Univ. of Milano Bicocca, Dept. Materials Science
dario.narducci@unimib.it

Outline

- Why «all silicon»
- Demo applications
- Redundancy
- Thermoelectric generators:
  - bottom-up
  - top-down
- Mechanical harvesting:
  - electrostatic
  - vibrational
- Batteries
- Some conclusions

Partners



9 partners
(E, I, BE, NL)

Coordinator:
CSIC
(IMB-CNM)

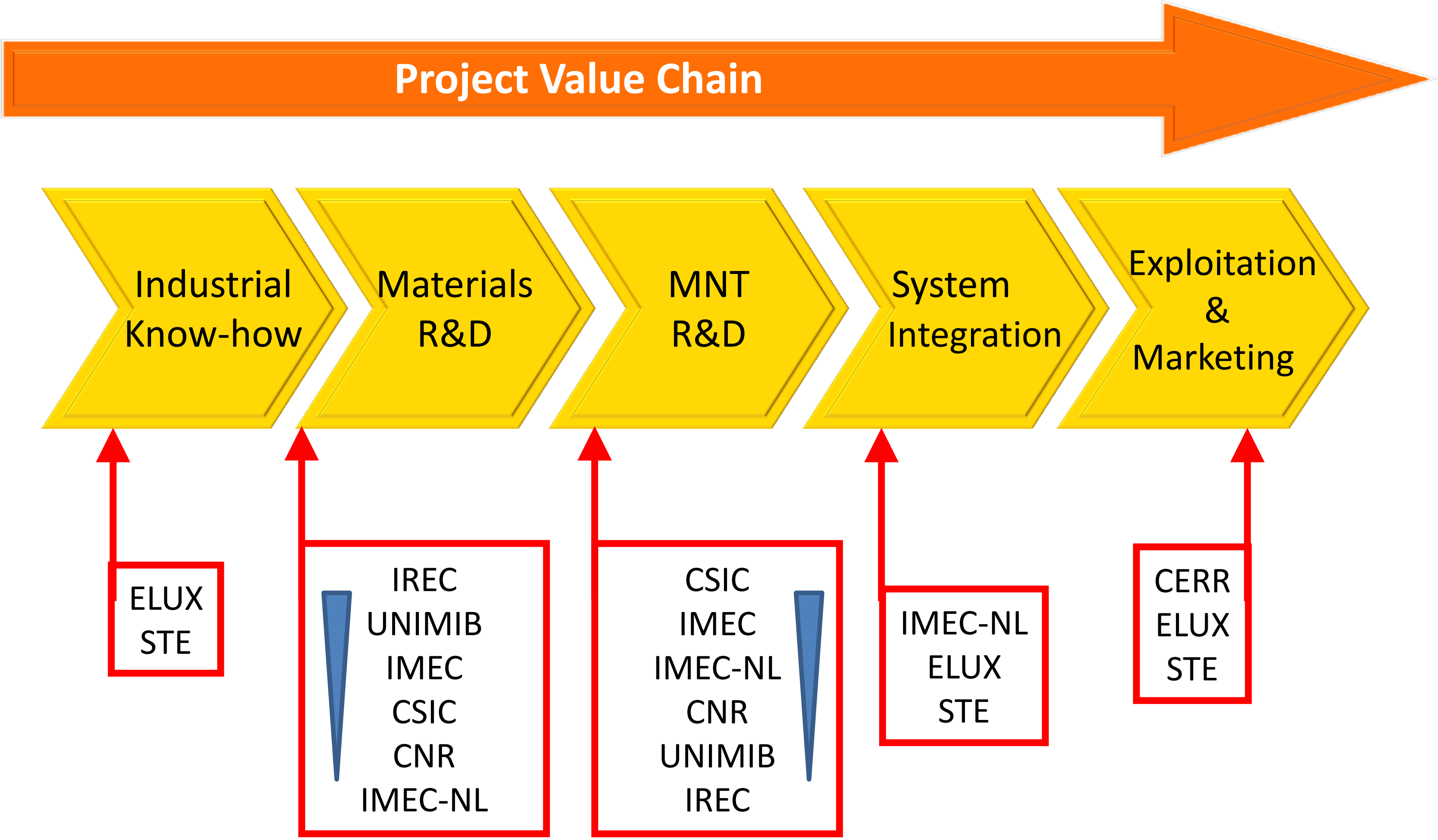
Why microenergy solutions: Replace primary batteries (cost, environmental, deployment flexibility issues) by harvesters + secondary batteries

Why Silicon materials and architectures: tap into the micro-nanoelectronics field which is an enabling technology, dealing with miniaturised and high density features (3D) implementations, offering economy of scale (serve mass markets) and the possibility of integration and addition of control and smartness

Why such applications: complementary microenergy testbeds from the perspective of silicon benefits ('smaller is better', 'cheaper is better') and availability of energy harvesting sources

Project value chain

Silicon Friendly Materials and Device Solutions
for Microenergy Applications



Project Value Chain

Industrial Know-how

Materials R&D

MNT R&D

System Integration

Exploitation & Marketing

ELUX
STE

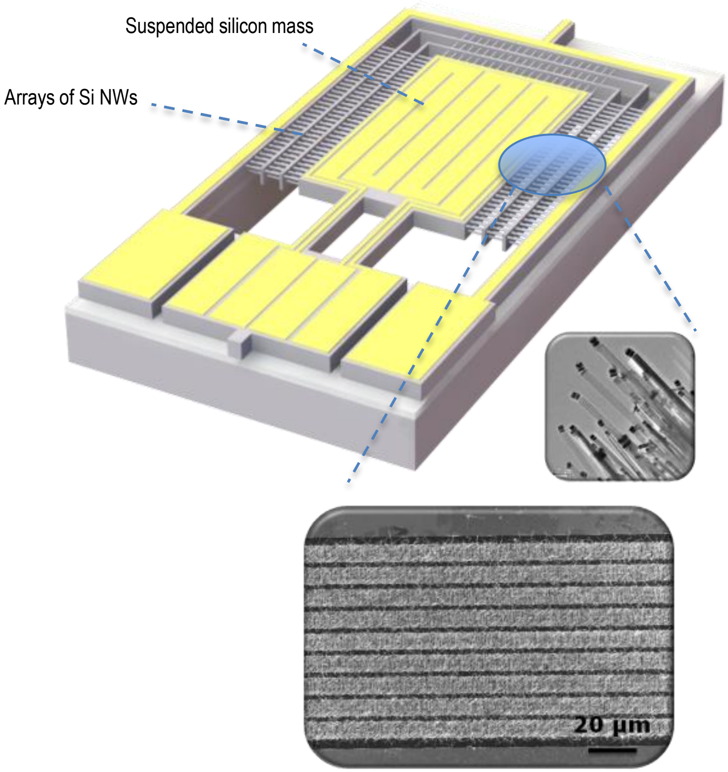
IREC
UNIMIB
IMEC
CSIC
CNR
IMEC-NL

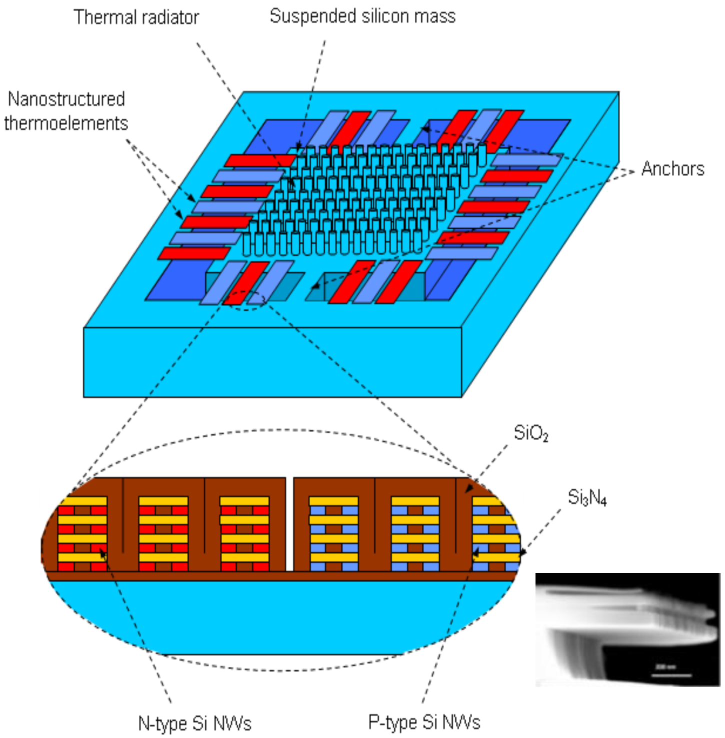
CSIC
IMEC
IMEC-NL
CNR
UNIMIB
IREC

IMEC-NL
ELUX
STE

CERR
ELUX
STE

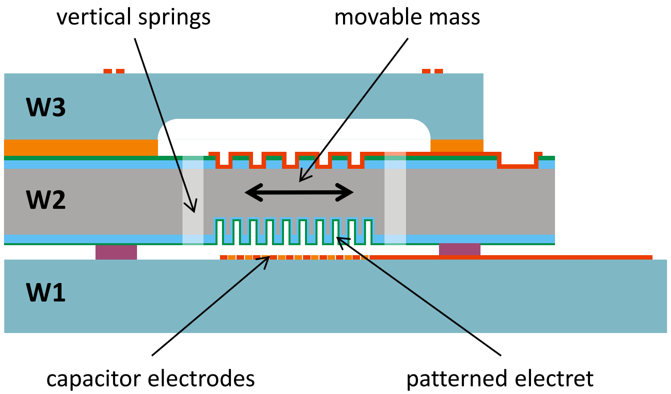
- 3D microstructures + bottom-up SiNWs
- 3D microstructures + top-down SiNWs

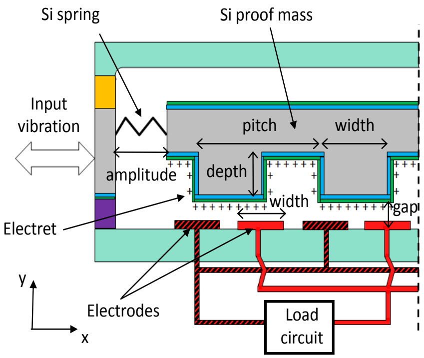




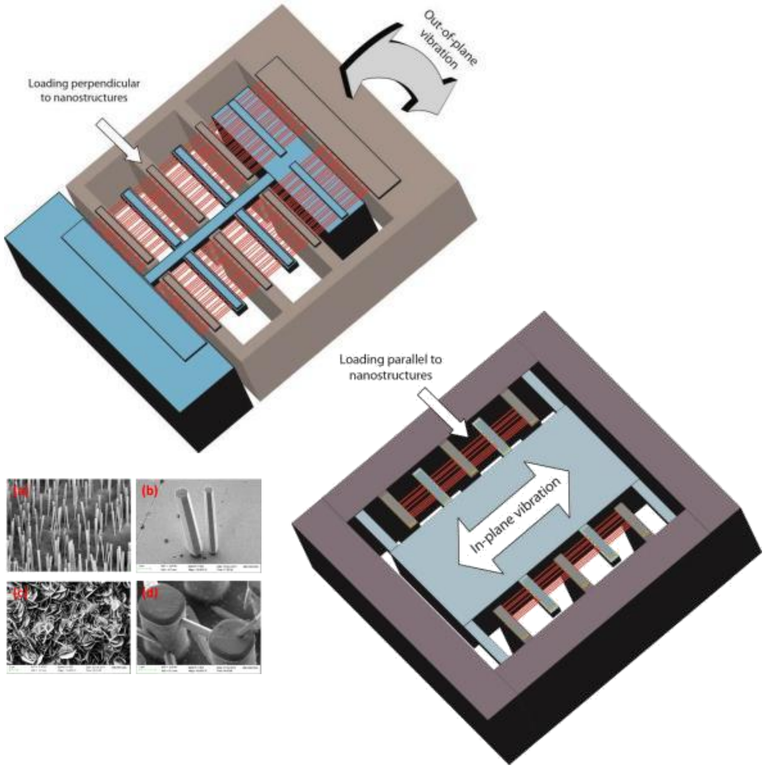
Mechanical harvesting

- 3D microstructures + electrostatic

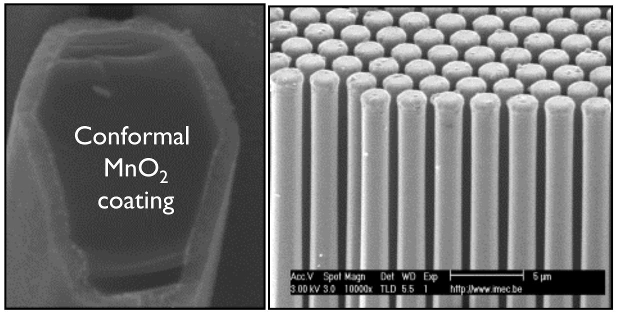




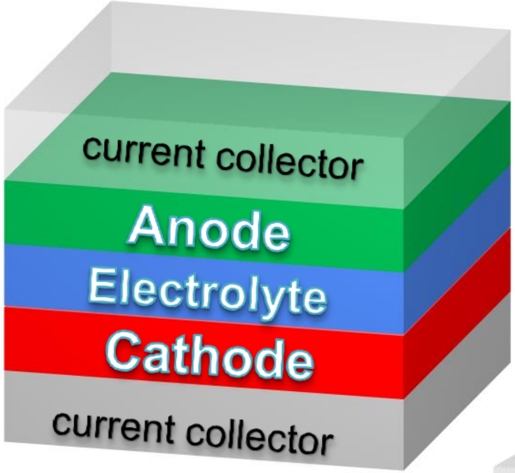
- 3D microstructures + piezoelectric



- Materials for Si compatible batteries
- 3D microstructures



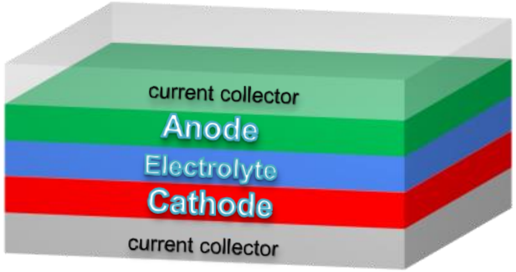
High capacity & power



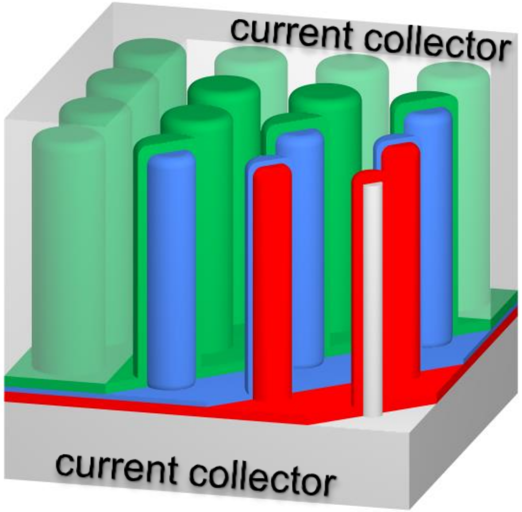
High capacity
Low power

Thin film

Low capacity
High power



3D



Application scenarios

Smart Pot

Cooking control
High-value niche market
Portable and adaptive

Test-bed for thermal harvesting

Tire Pressure monitoring

Intelligent tire
Large market volume
Small size

Test-bed for vibration harvesting

Predictive maintenance

Rotating-reciprocating machines
Large shop floors
High number of nodes
Difficult servicing

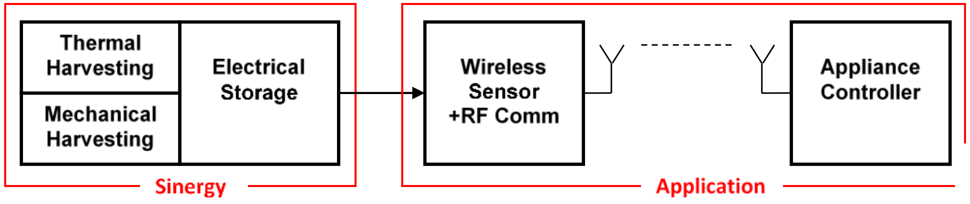
Test-bed for vibration and thermal harvesting

Is technology at least potentially adequate?

- Predictive maintenance/domestic application system
  - Thermal harvester requirements under application conditions
  - Sensor system architecture
  - Planning/choice of application demonstrator
- Tire Pressure Monitoring Systems (TPMS)
  - Vibration harvester performance under application conditions
  - TPMS architecture
  - Planning

Domestic appliances

- Food temperature in pots: 80-250 °C
- Transmit temperature to HOB



Thermal Harvesting

Mechanical Harvesting

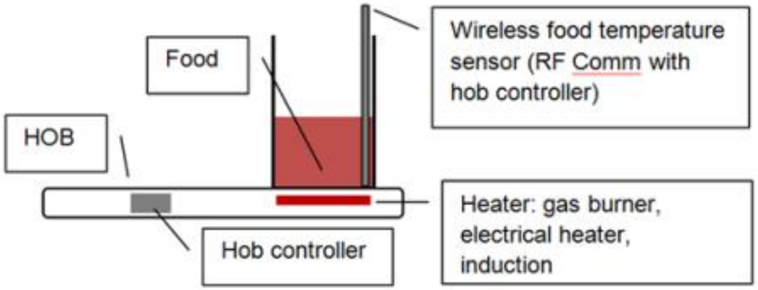
Electrical Storage

Sinergy

Wireless Sensor +RF Comm

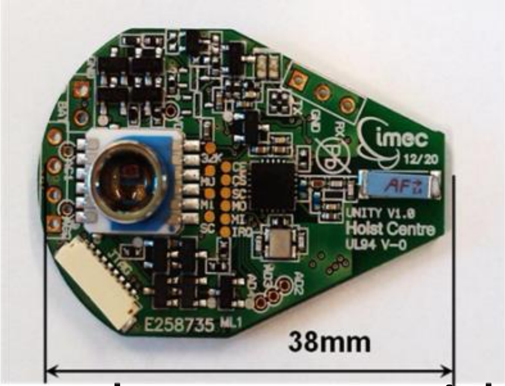
Appliance Controller

Application



Predictive maintenance

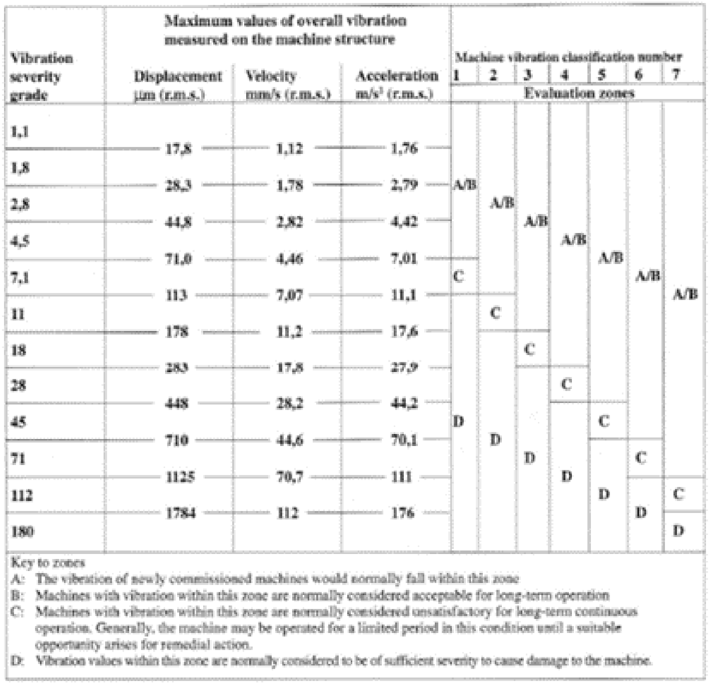
- Sensors: temperature, acceleration
- Reuse sensor system from IMEC and add new sensors (low power acceleration/temperature sensors) with programmable logic



- Preference is thermal energy harvester with off the shelf power management IC

Exploration of a combined system - Integration strategy

- Machine guide values
  - displacements in the operational ranges 17.8 – 1125 µm (rms);
  - velocity in the operational ranges 1.12 – 70.7 mm/s (rms);
  - acceleration in the operational ranges 1.76 – 111 m/s^2 (rms);
  - Temperature range: 10-60 ^{o}C



Vibration severity grade	Maximum values of overall vibration measured on the machine structure			Machine vibration classification number						
	Displacement µm (r.m.s.)	Velocity mm/s (r.m.s.)	Acceleration m/s² (r.m.s.)	1	2	3	4	5	6	7
				Evaluation zones						
1,1	17,8	1,12	1,76	A/B	A/B	A/B	A/B	A/B	A/B	A/B
1,8	28,3	1,78	2,79							
2,8	44,8	2,82	4,42							
4,5	71,0	4,46	7,01							
7,1	113	7,07	11,1	C						
11	178	11,2	17,6	D	C					
18	283	17,8	27,9		D	C				
28	448	28,2	44,2			D	C			
45	710	44,6	70,1				D	C		
71	1125	70,7	111					D	C	
112	1784	112	176						D	C
180										D

Key to zones
A: The vibration of newly commissioned machines would normally fall within this zone
B: Machines with vibration within this zone are normally considered acceptable for long-term operation
C: Machines with vibration within this zone are normally considered unsatisfactory for long-term continuous operation. Generally, the machine may be operated for a limited period in this condition until a suitable opportunity arises for remedial action.
D: Vibration values within this zone are normally considered to be of sufficient severity to cause damage to the machine.

Table 2.8 Vibration classification numbers and guide values for reciprocating machines. (ISO 10816-6)

Thermoeletric harvesters

Strategy and device layouts

Goal: Obtain all-silicon thermoelectric micronanogenerators by means of the integration of silicon based NW arrays (as thermoelectric material) into a Si micromachined structure able to exploit a waste heat source to develop an internal thermal contrast between two isolated silicon parts.

Bottom-up strategy – Device layout

NWs will be grown with a VLS-CVD method that allows the in-situ integration of large density arrays of NWs within a 3D structure without specific nanolithography techniques.

Process workflow

- Deposition of gold nanoparticles on device trenches by Galvanic Displacement

⇩

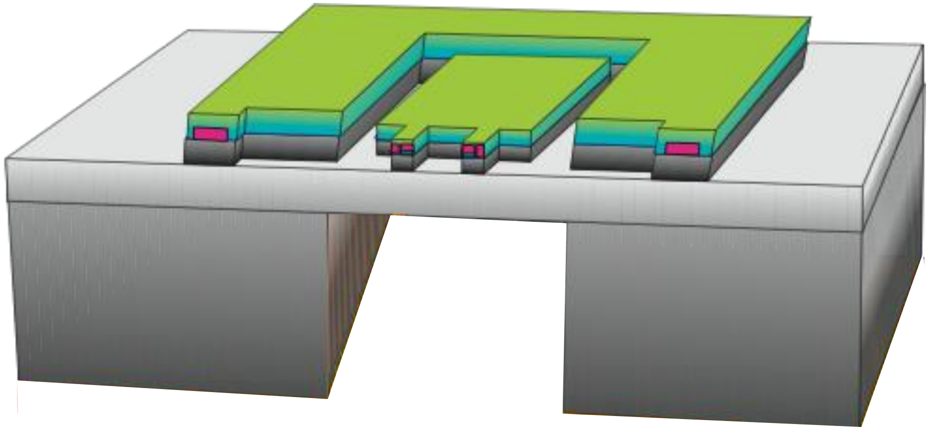
- Growth of silicon nanowires on CVD by VLS synthesis

⇩

- Removal of membrane and passivation oxide with HF

⇩

- Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

Process workflow

- Deposition of gold nanoparticles on device trenches by Galvanic Displacement

⇩

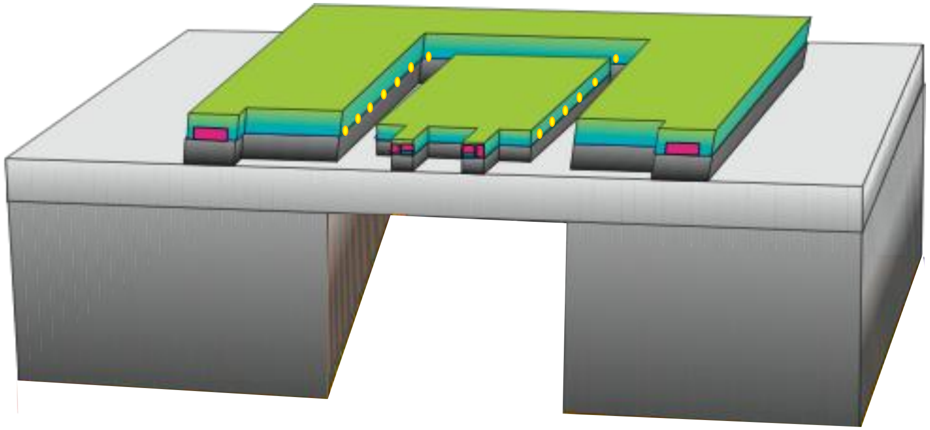
- Growth of silicon nanowires on CVD by VLS synthesis

⇩

- Removal of membrane and passivation oxide with HF

⇩

- Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

Process workflow

- ⊙ Deposition of gold nanoparticles on device trenches by Galvanic Displacement

⇩

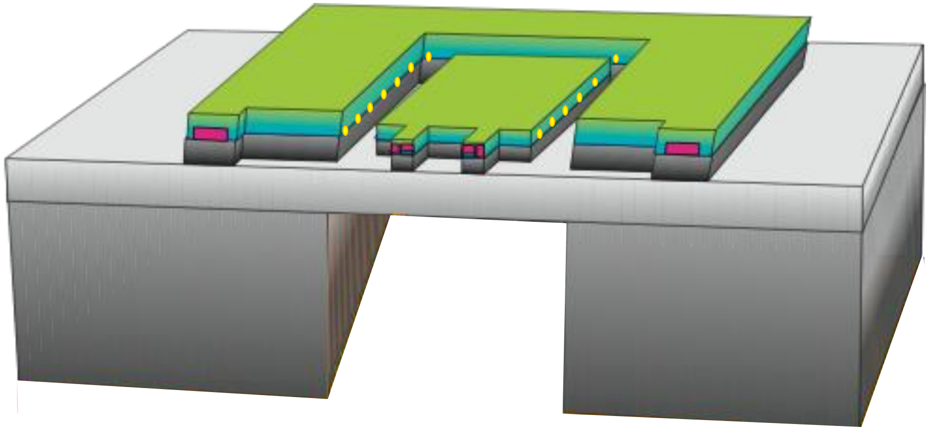
- ⊙ Growth of silicon nanowires on CVD by VLS synthesis

⇩

- Removal of membrane and passivation oxide with HF

⇩

- Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

Process workflow

- Deposition of gold nanoparticles on device trenches by Galvanic Displacement

⇩

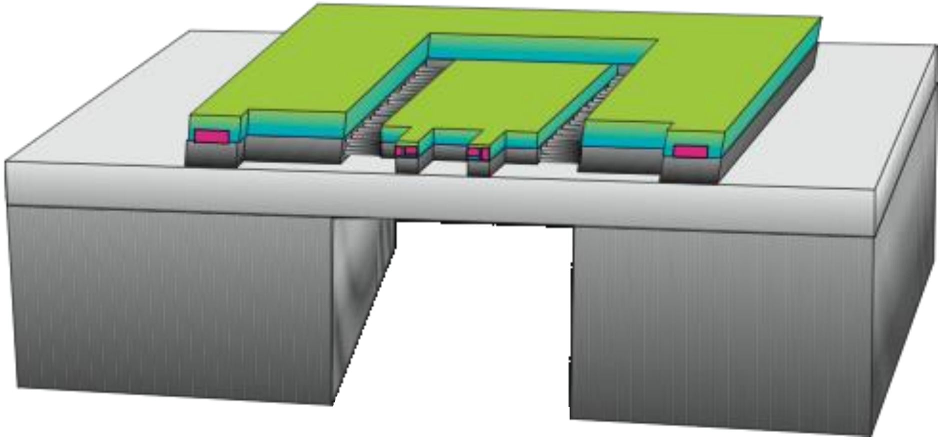
⊙ Growth of silicon nanowires on CVD by VLS synthesis

⇩

- Removal of membrane and passivation oxide with HF

⇩

- Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

Process workflow

- Deposition of gold nanoparticles on device trenches by Galvanic Displacement

⇩

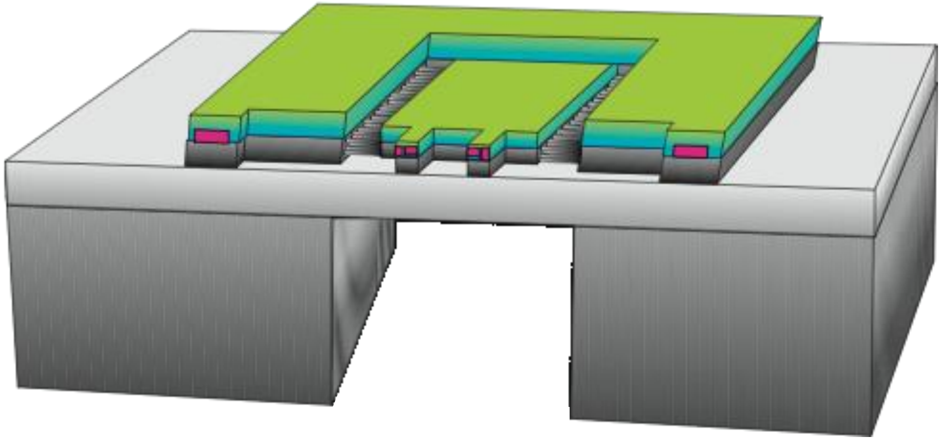
⊙ Growth of silicon nanowires on CVD by VLS synthesis

⇩

⊙ Removal of membrane and passivation oxide with HF

⇩

⊙ Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

Process workflow

- Deposition of gold nanoparticles on device trenches by Galvanic Displacement

⇩

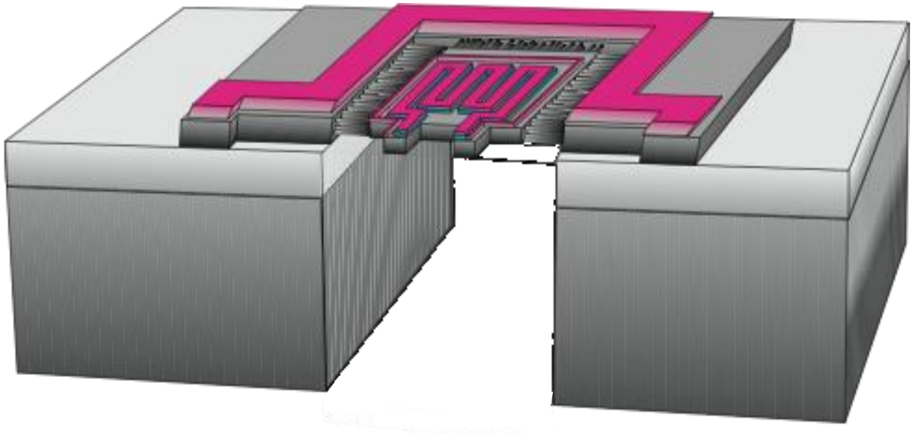
- Growth of silicon nanowires on CVD by VLS synthesis

⇩

⊙ Removal of membrane and passivation oxide with HF

⇩

⊙ Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

Microemulsion Galvanic Displacement

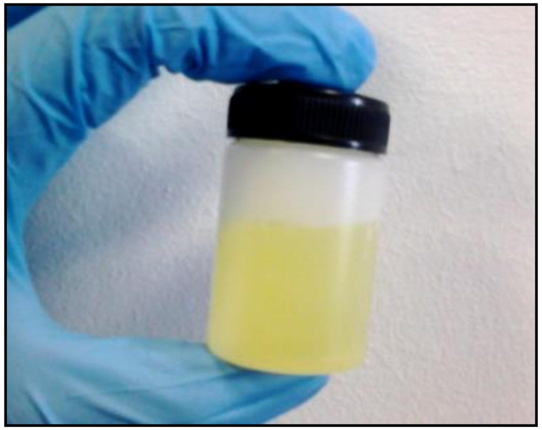
1 – Several **microemulsions** with different R values are **prepared**.

Aqueous phase: 0.2M HF + 0.01M $KAuCl_4$

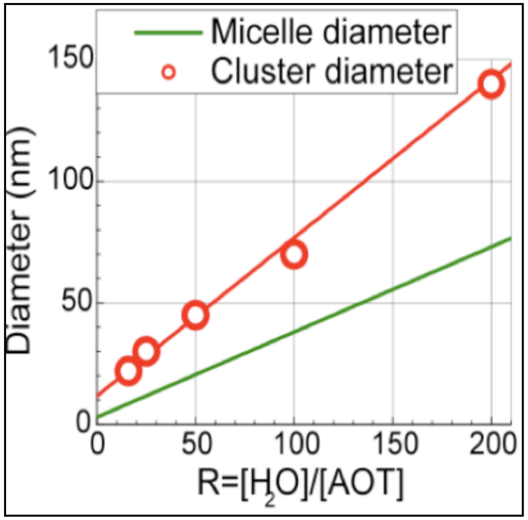
+

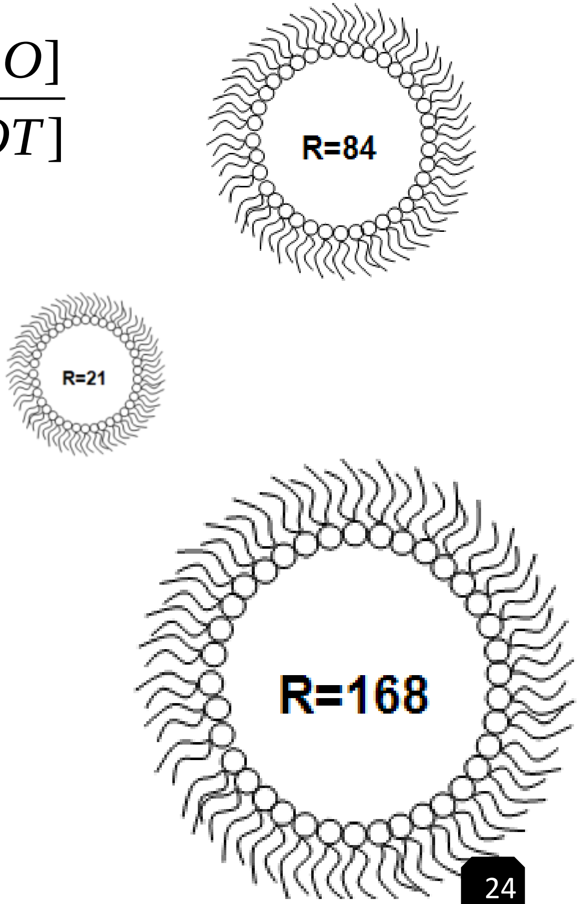
Organic phase: 0.33M AOT (surfactant) in n-heptane

↓



$$R=\frac{[\text{Water}]}{[\text{Surfactant}]}=\frac{[H_2O]}{[AOT]}$$





Gao et al, J. Am. Chem. Soc. 127, 4574 (2005)

Microemulsion Galvanic Displacement

1 – Several **microemulsions** with different R values are **prepared**.

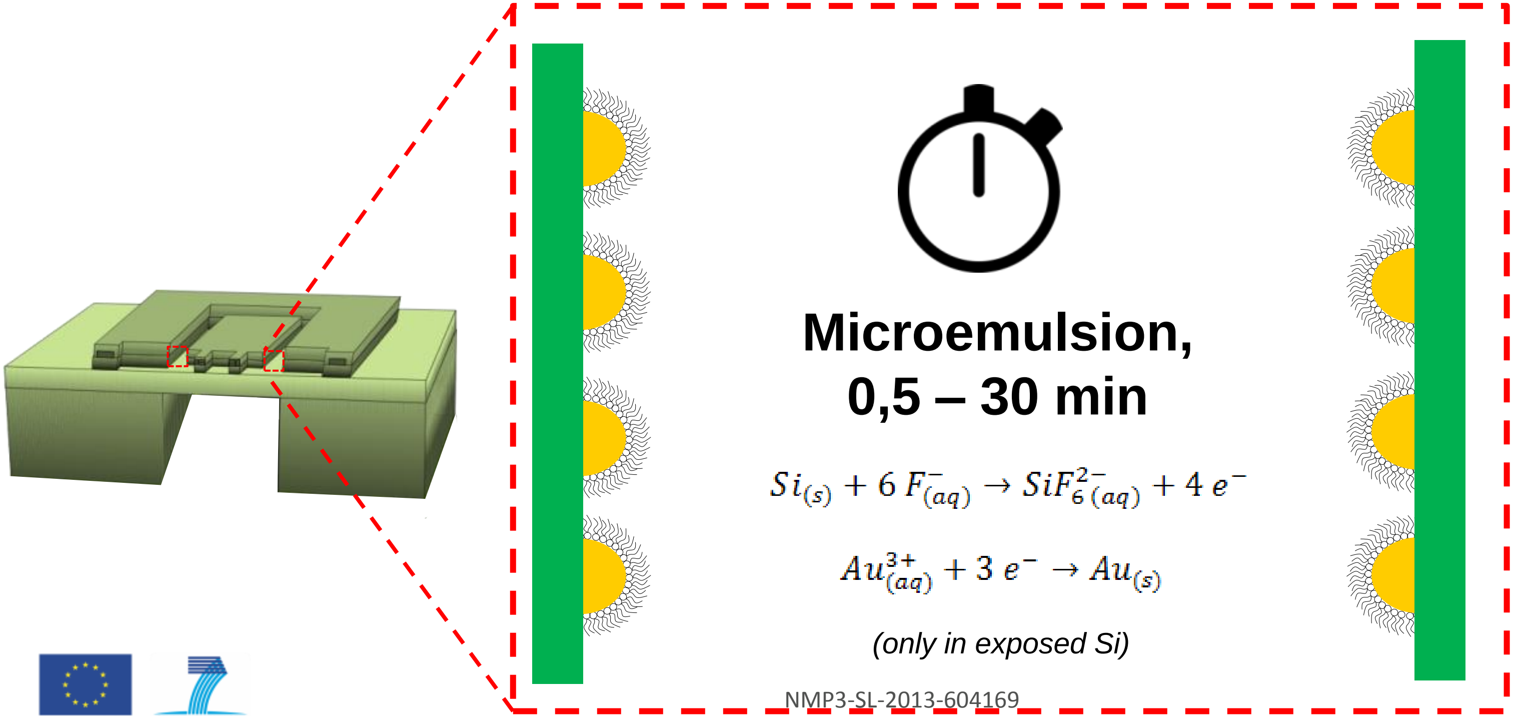
2 – Devices are **dipped in HF** in order to remove native oxide from trenches

Microemulsion Galvanic Displacement

1 – Several **microemulsions** with different R values are **prepared**.

2 – Devices are **dipped in HF** in order to remove native oxide from trenches

3 – Devices are **dipped in microemusions** during a controlled dipping time. Gold NPs are formed



**Microemulsion,
0,5 – 30 min**

$$Si_{(s)} + 6\,F^-_{(aq)} \rightarrow SiF^{2-}_{6\,(aq)} + 4\,e^-$$

$$Au^{3+}_{(aq)} + 3\,e^- \rightarrow Au_{(s)}$$

(only in exposed Si)

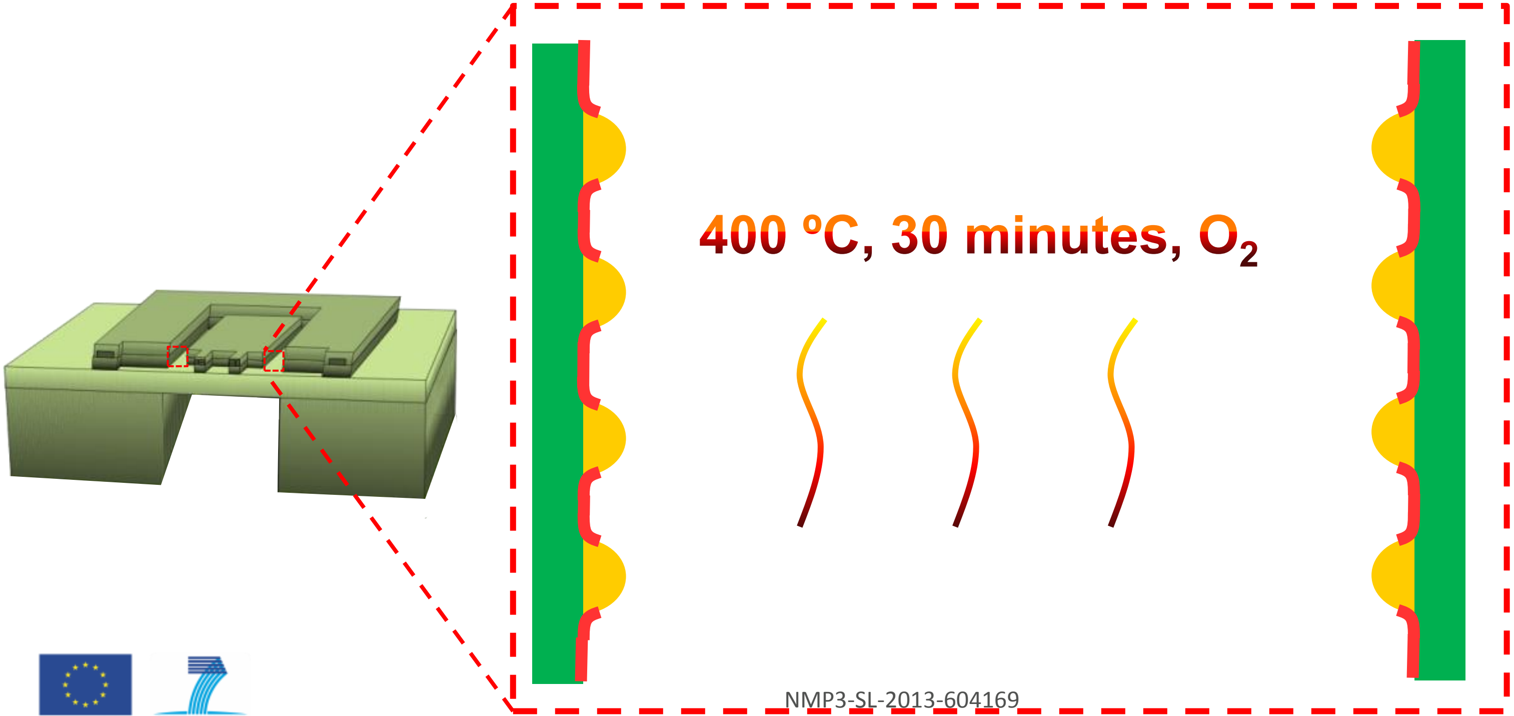
Microemulsion Galvanic Displacement

1 – Several **microemulsions** with different R values are **prepared**.

2 – Devices are **dipped in HF** in order to remove native oxide from trenches

3 – Devices are **dipped in microemusions** during a controlled dipping time. Gold NPs are formed

4 – Devices are **annealed** to remove the remaining surfactant



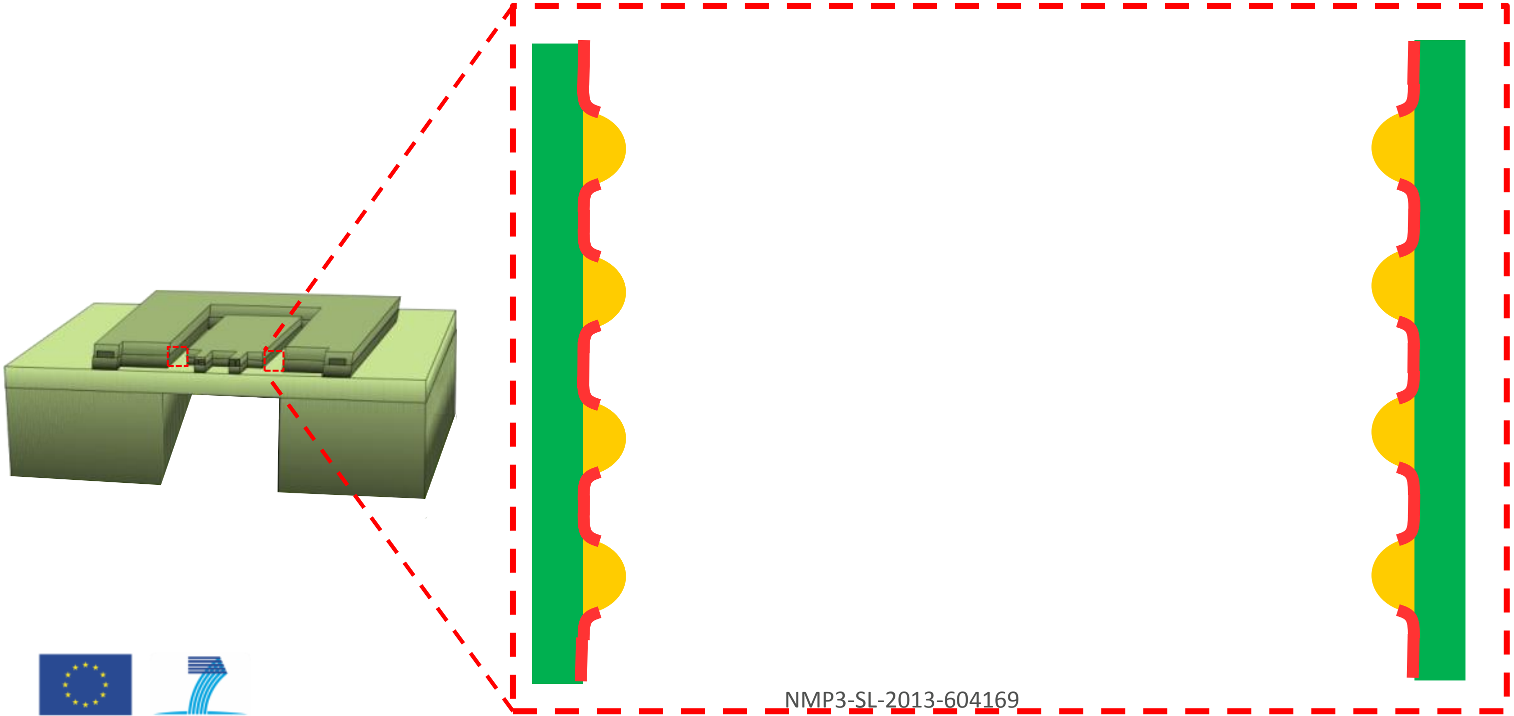
Microemulsion Galvanic Displacement

1 – Several **microemulsions** with different R values are **prepared**.

2 – Devices are **dipped in HF** in order to remove native oxide from trenches

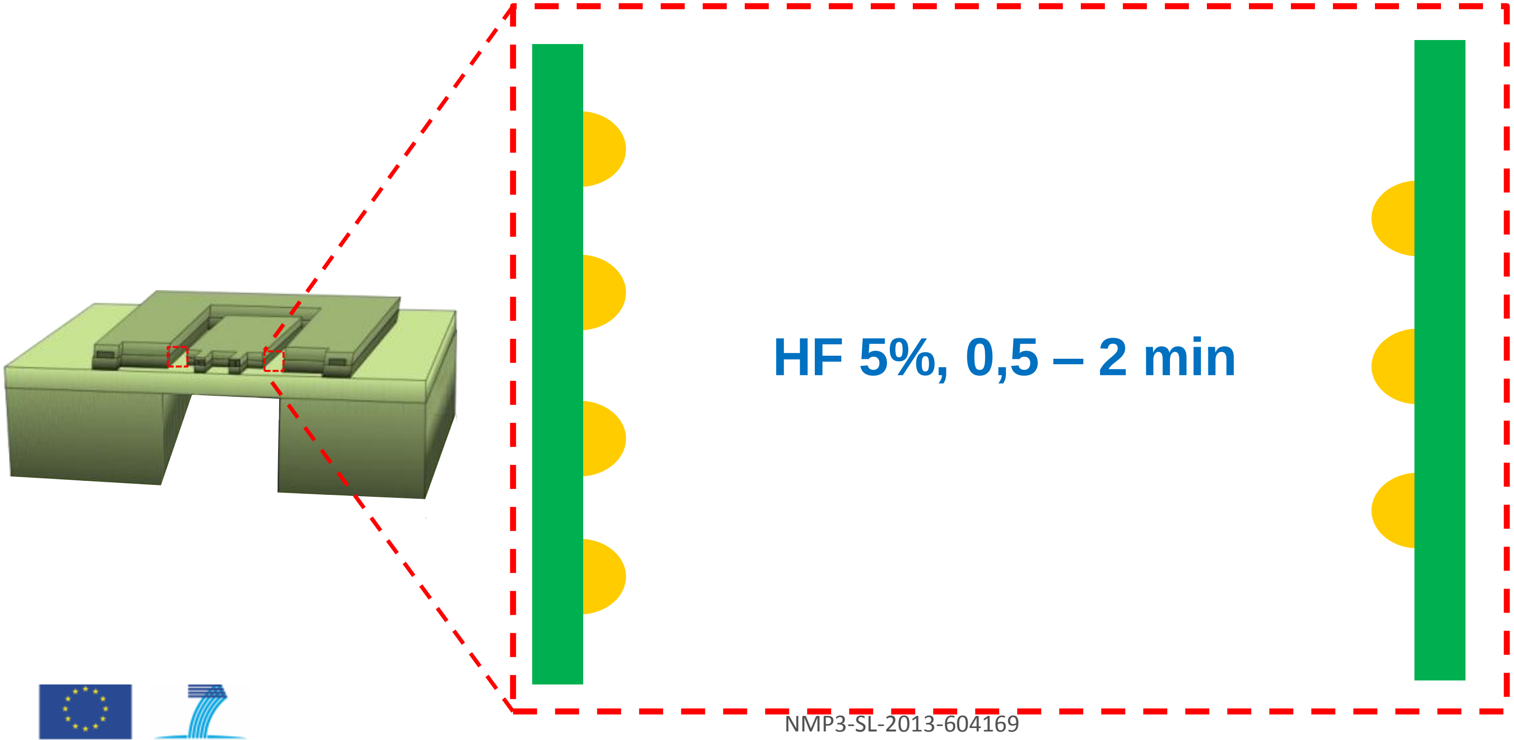
3 – Devices are **dipped in microemusions** during a controlled dipping time. Gold NPs are formed

4 – Devices are **annealed** to remove the remaining surfactant



CVD-VLS growth of silicon nanowires

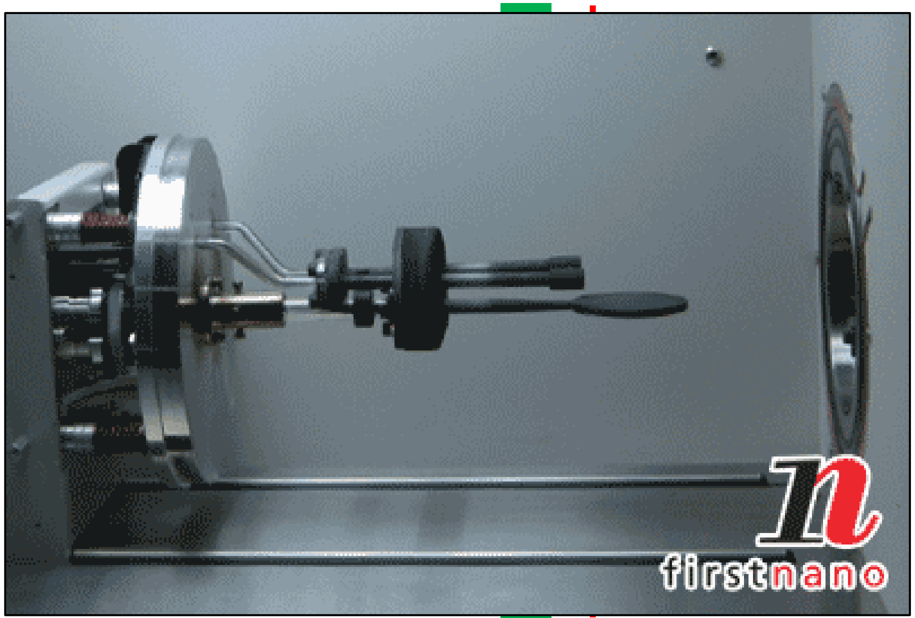
1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination


HF 5%, 0,5 – 2 min

CVD-VLS growth of silicon nanowires

1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination

2 – Devices are loaded into **CVD**

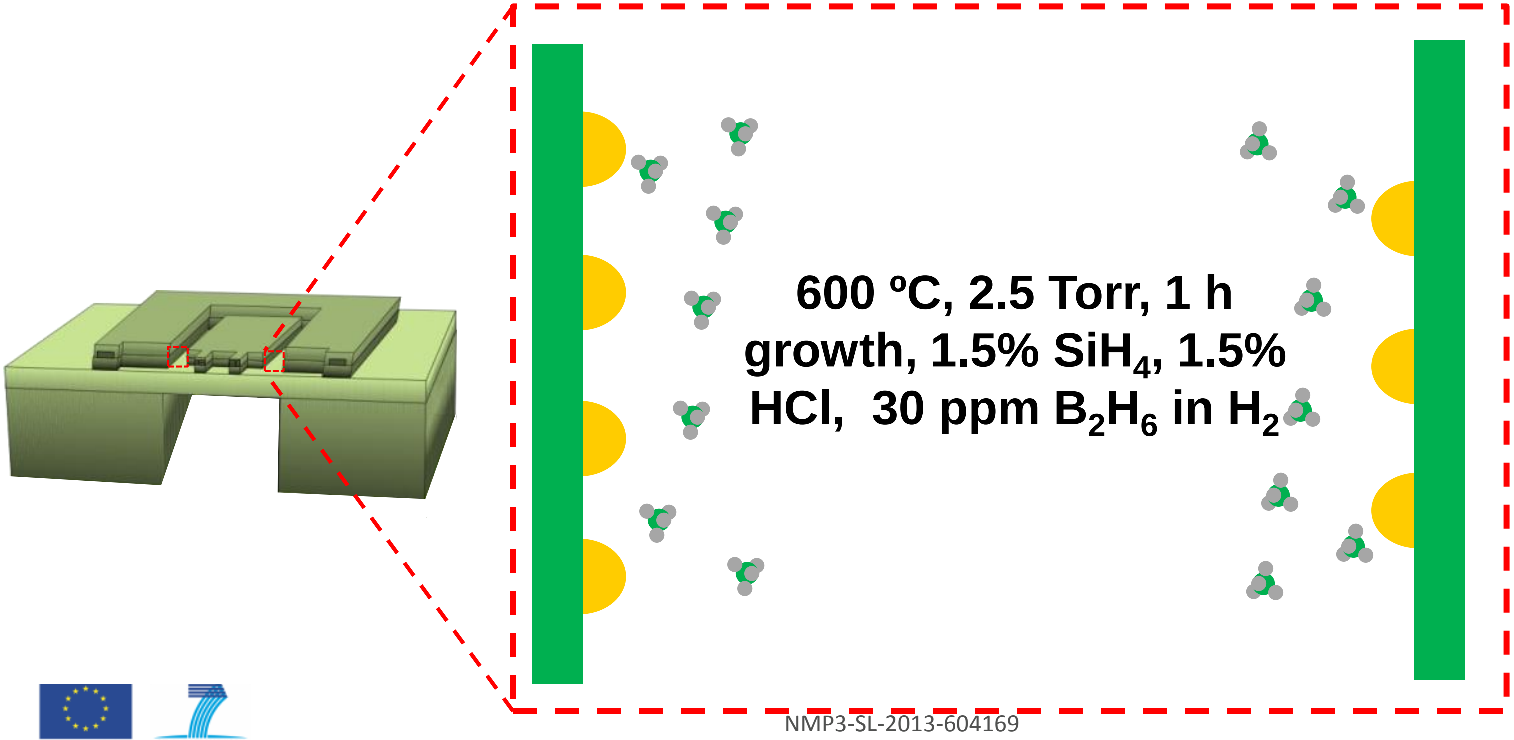


CVD-VLS growth of silicon nanowires

1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination

2 – Devices are loaded into **CVD**

3 – There devices are brought to **reaction conditions and exposed to silane.** Silicon nanowires are grown by VLS synthesis



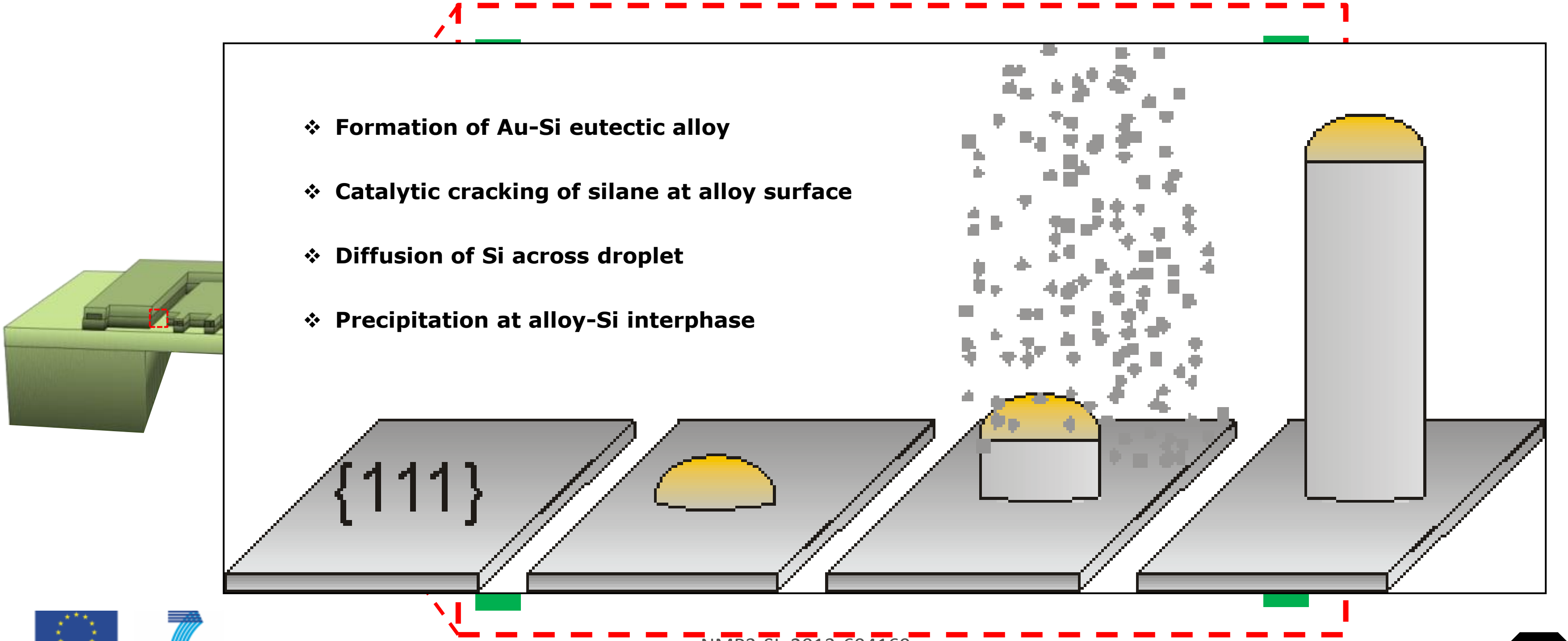
600 ºC, 2.5 Torr, 1 h growth, 1.5% SiH_4, 1.5% HCl, 30 ppm B_2H_6 in H_2

CVD-VLS growth of silicon nanowires

1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination

2 – Devices are loaded into **CVD**

3 – There devices are brought to **reaction conditions and exposed to silane.** Silicon nanowires are grown by VLS synthesis



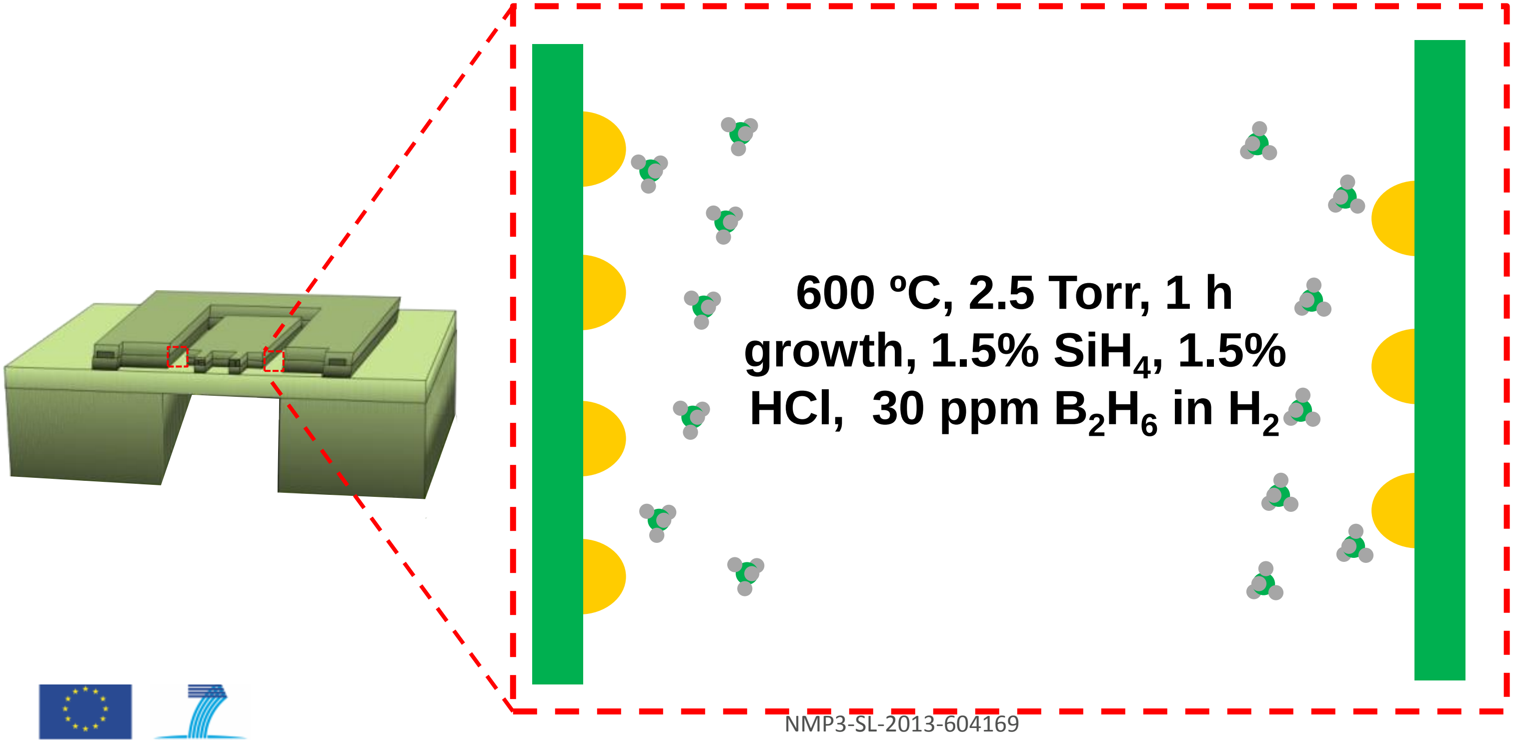
- **Formation of Au-Si eutectic alloy**
- **Catalytic cracking of silane at alloy surface**
- **Diffusion of Si across droplet**
- **Precipitation at alloy-Si interphase**

CVD-VLS growth of silicon nanowires

1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination

2 – Devices are loaded into **CVD**

3 – There devices are brought to **reaction conditions and exposed to silane.** Silicon nanowires are grown by VLS synthesis



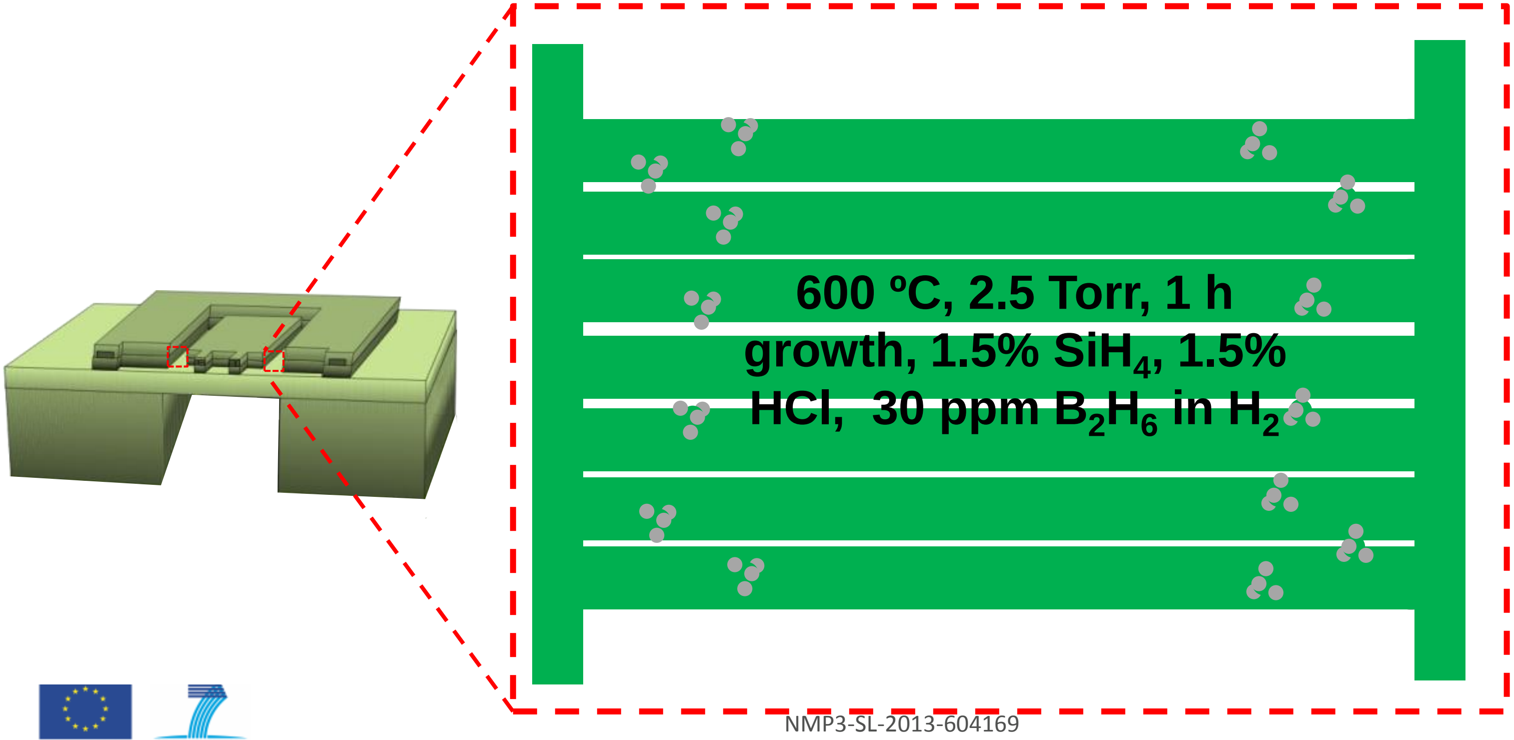
600 ºC, 2.5 Torr, 1 h growth, 1.5% SiH_4, 1.5% HCl, 30 ppm B_2H_6 in H_2

CVD-VLS growth of silicon nanowires

1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination

2 – Devices are loaded into **CVD**

3 – There devices are brought to **reaction conditions and exposed to silane.** Silicon nanowires are grown by VLS synthesis



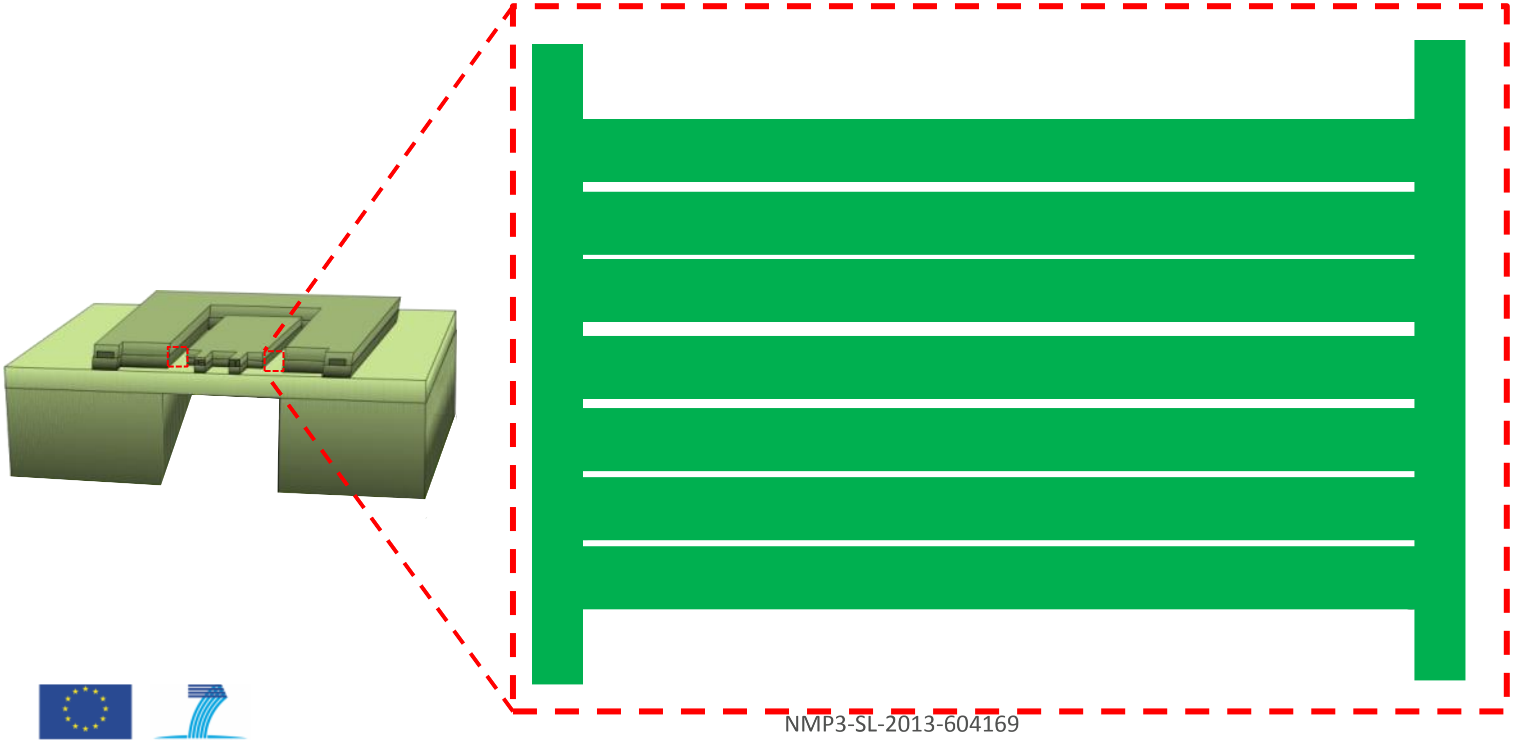
600 ºC, 2.5 Torr, 1 h growth, 1.5% SiH_4, 1.5% HCl, 30 ppm B_2H_6 in H_2

CVD-VLS growth of silicon nanowires

1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination

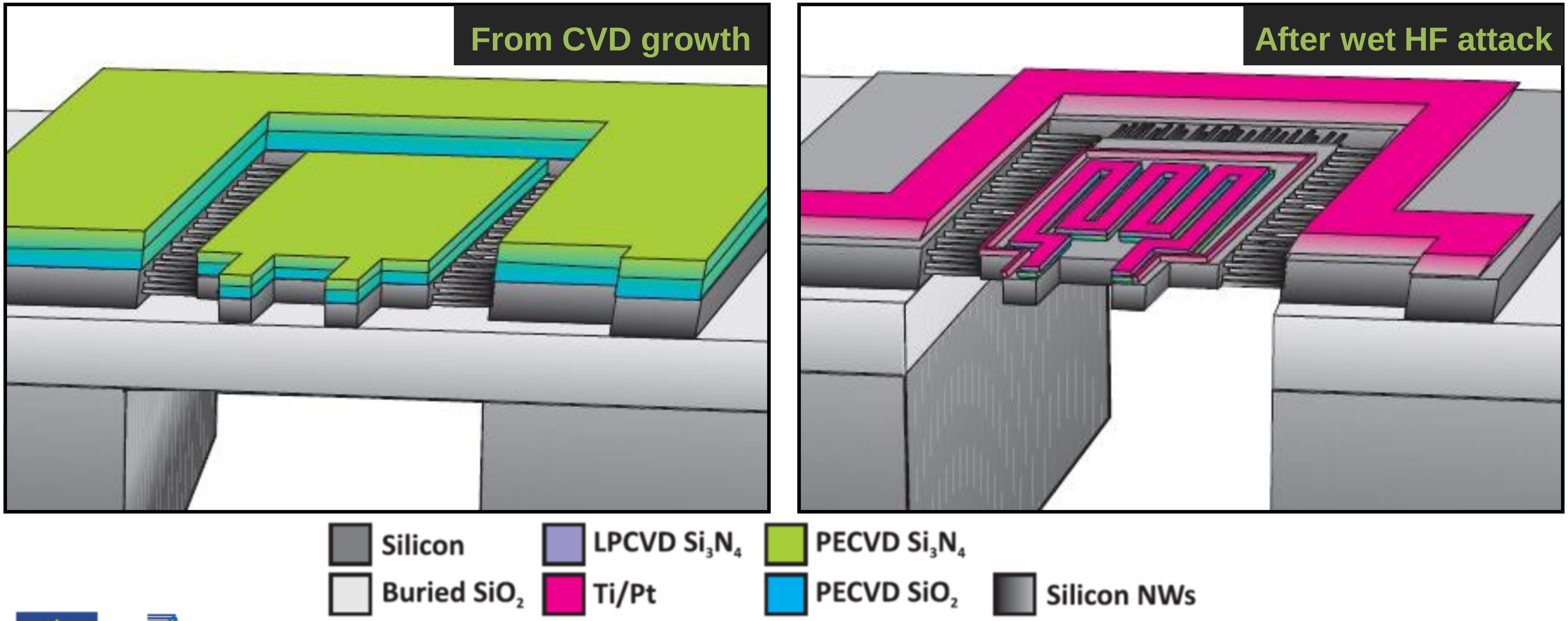
2 – Devices are loaded into **CVD**

3 – There devices are brought to **reaction conditions and exposed to silane**. Silicon nanowires are grown by VLS synthesis



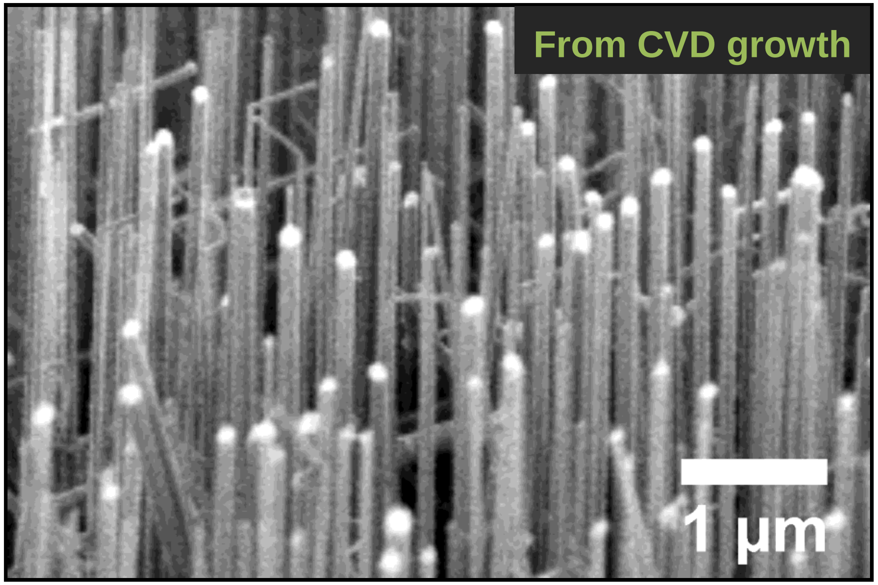
Membrane removal in HF

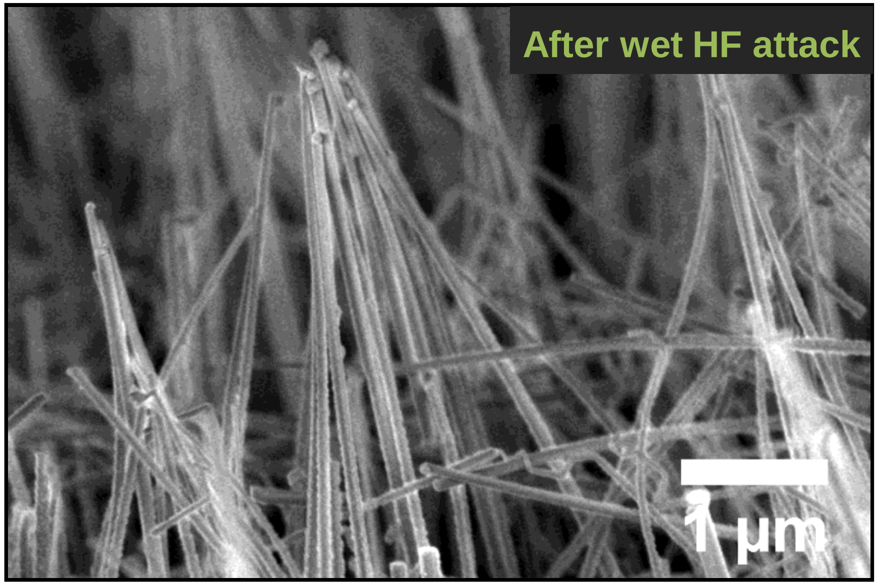
After growing Si NWs in a µTEG device a wet attack in HF must be performed in order to remove membrane and passivation silicon oxide – which covers contacts.



Membrane removal in HF

After growing Si NWs in a µTEG device a wet attack in HF must be performed in order to remove membrane and passivation silicon oxide – which covers contacts.

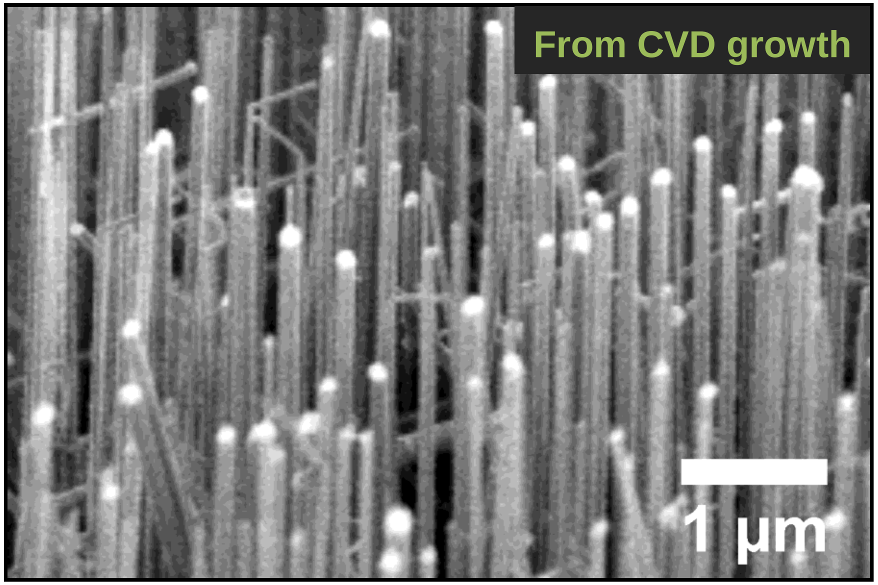

From CVD growth

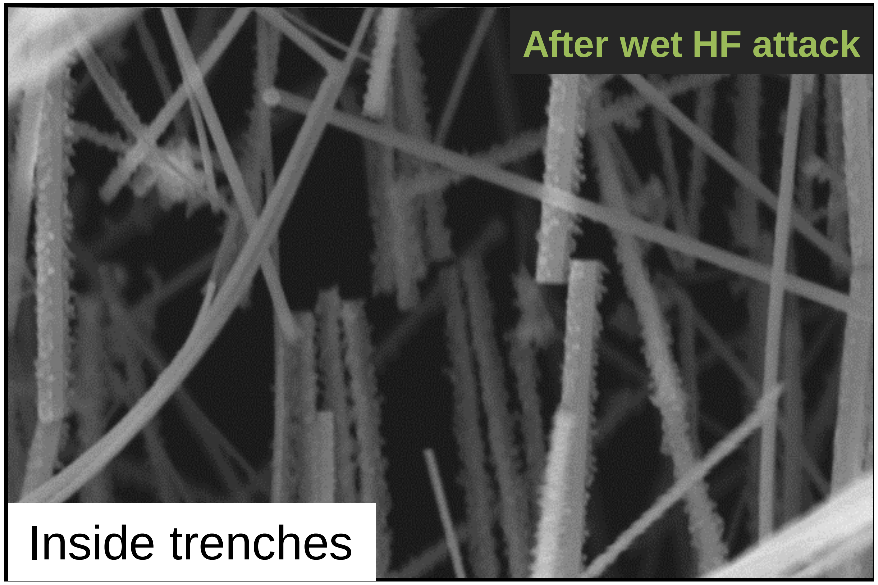

After wet HF attack

⬛ Silicon
▢ Buried SiO_2
▨ LPCVD Si_3N_4
🟥 Ti/Pt
🟩 PECVD Si_3N_4
🟦 PECVD SiO_2
▨ Silicon NWs

Membrane removal in HF

After growing Si NWs in a µTEG device a wet attack in HF must be performed in order to remove membrane and passivation silicon oxide – which covers contacts.


From CVD growth


After wet HF attack

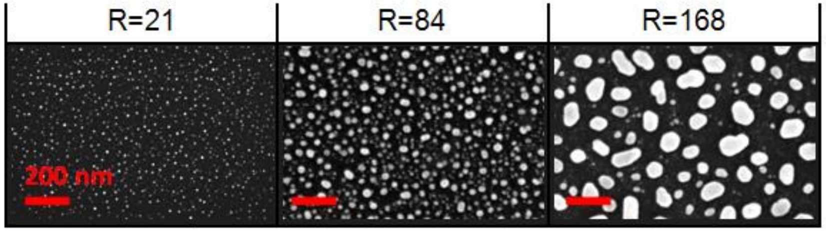
Inside trenches

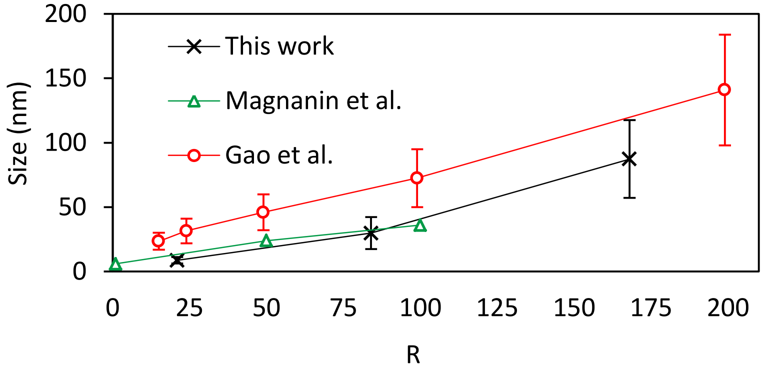
⬛ Silicon
🟪 LPCVD Si_3N_4
🟩 PECVD Si_3N_4
⬜ Buried SiO_2
🟥 Ti/Pt
🟦 PECVD SiO_2
▨ Silicon NWs

Galvanic Displacement – Catalyst control

- Effects of **R** of the microemulsion

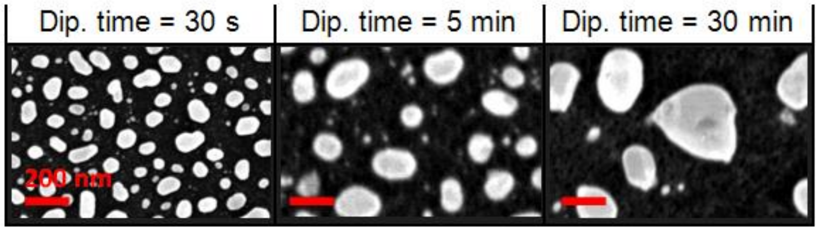
(30 s dipping)

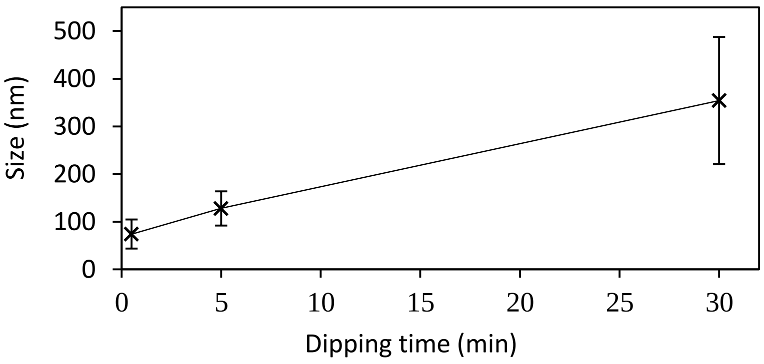




- Effects of **dipping time** in the microemulsion

(R=168)



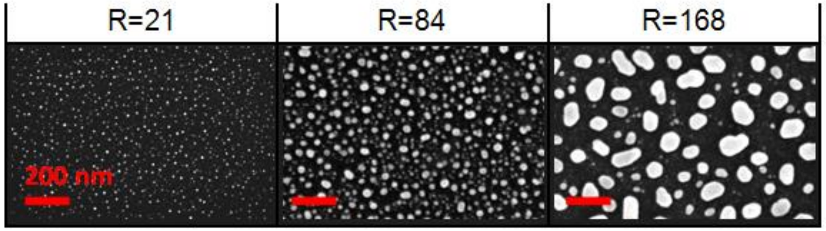


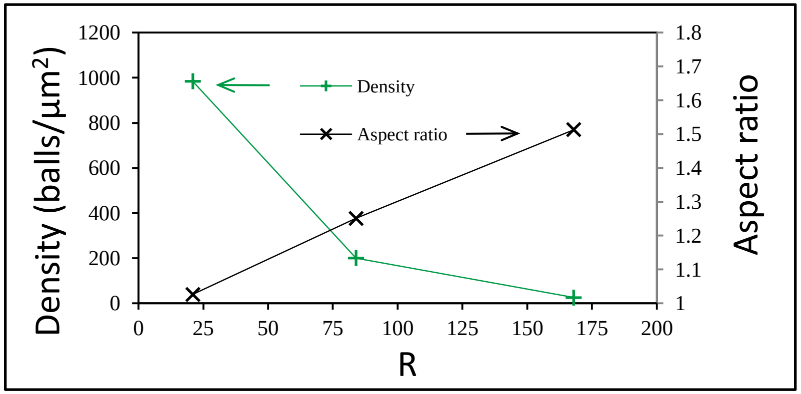
❖**Au NPs size increases with R and dipping time**

Galvanic Displacement – Catalyst control

- Effects of **R** of the microemulsion

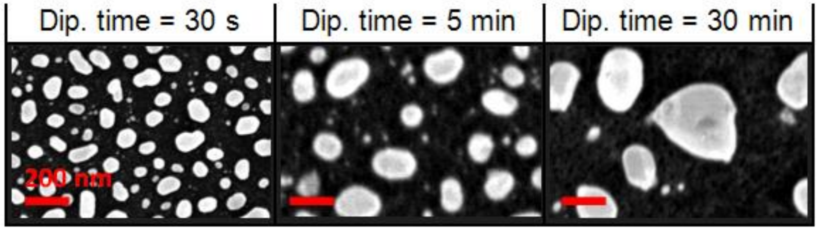
(30 s dipping)

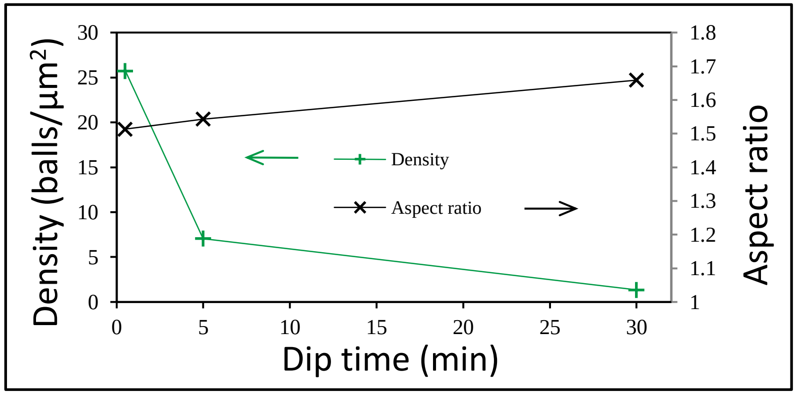




- Effects of **dipping time** in the microemulsion

(R=168)





❖**Au NPs size increases with R and dipping time**

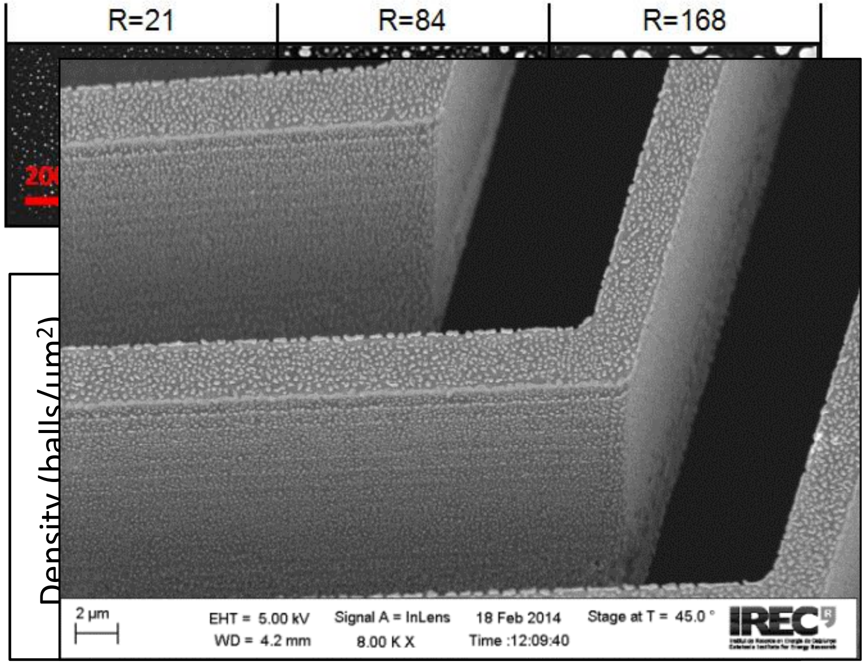
❖**Density decreases with R and dipping time**

European Union
SEVENTH FRAMEWORK PROGRAMME

Galvanic Displacement – Catalyst control

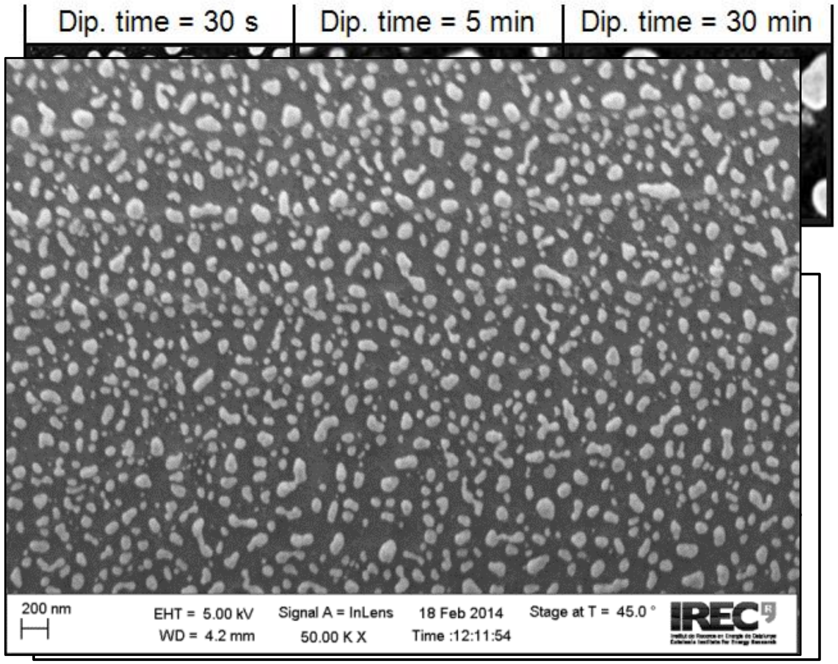
- Effects of **R** of the microemulsion

(30 s dipping)



- Effects of **dipping time** in the microemulsion

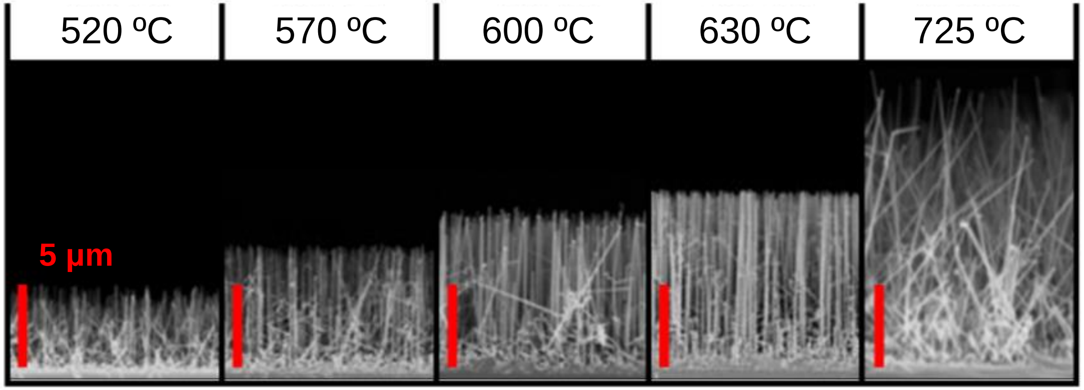
(R=168)



❖**Au NPs size increases with R and dipping time**

❖**Density decreases with R and dipping time**

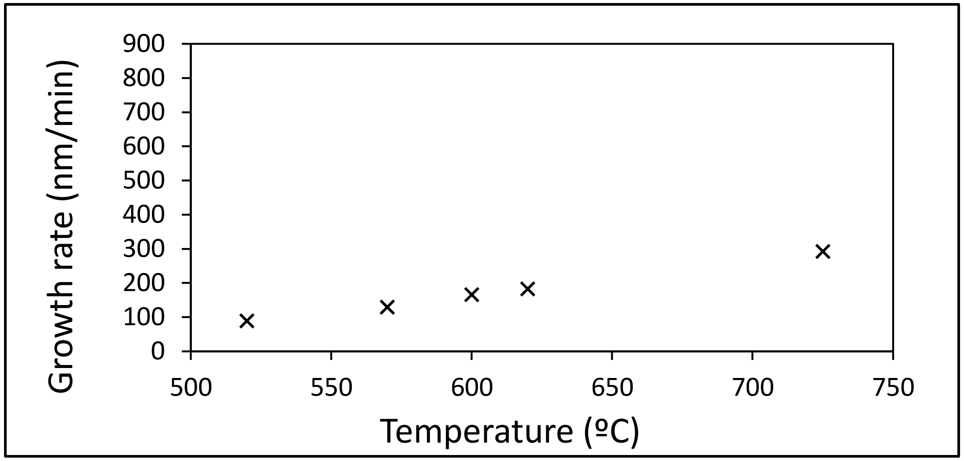
CVD-VLS – Nanowire control – Effect of temperature



R168

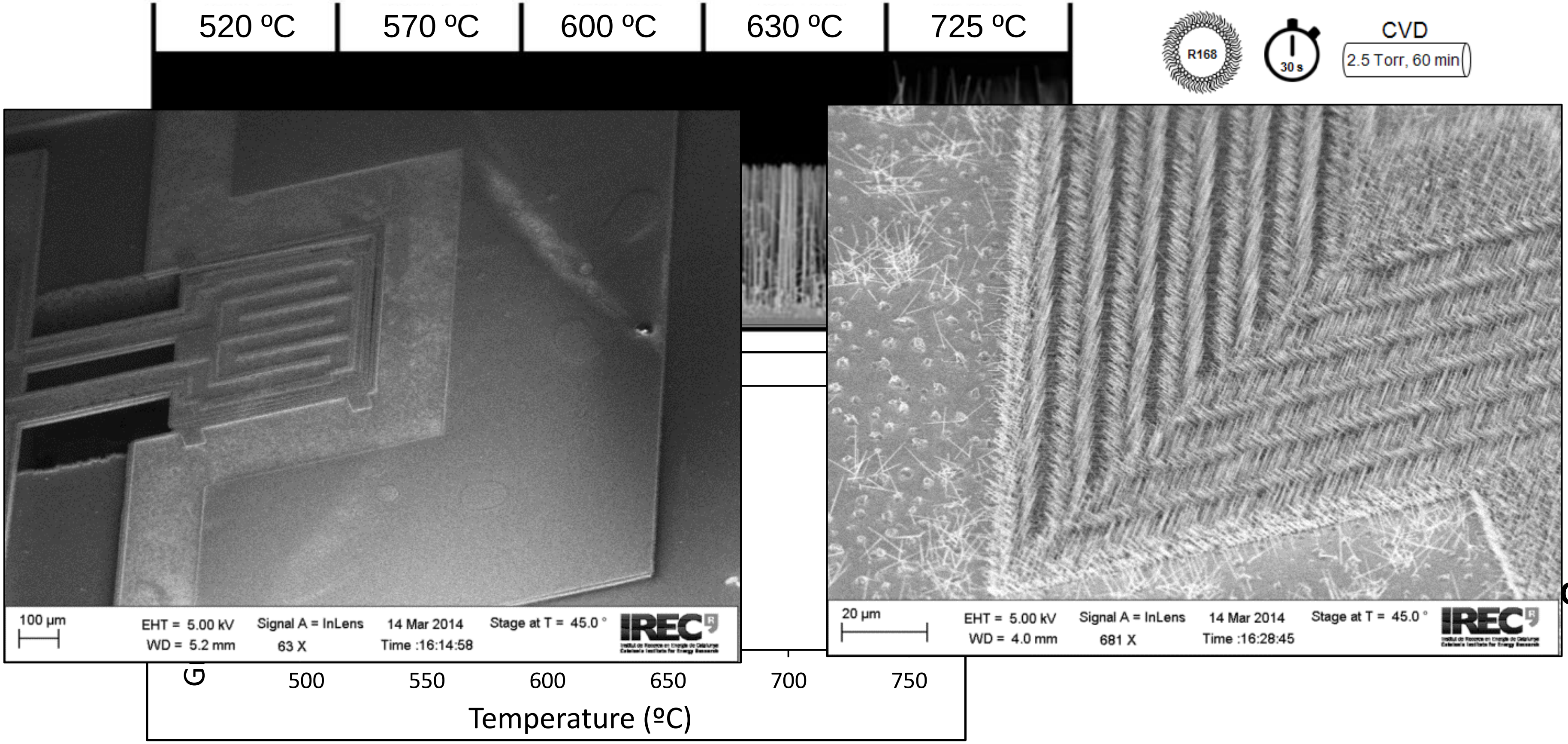
30 s

CVD
2.5 Torr, 60 min



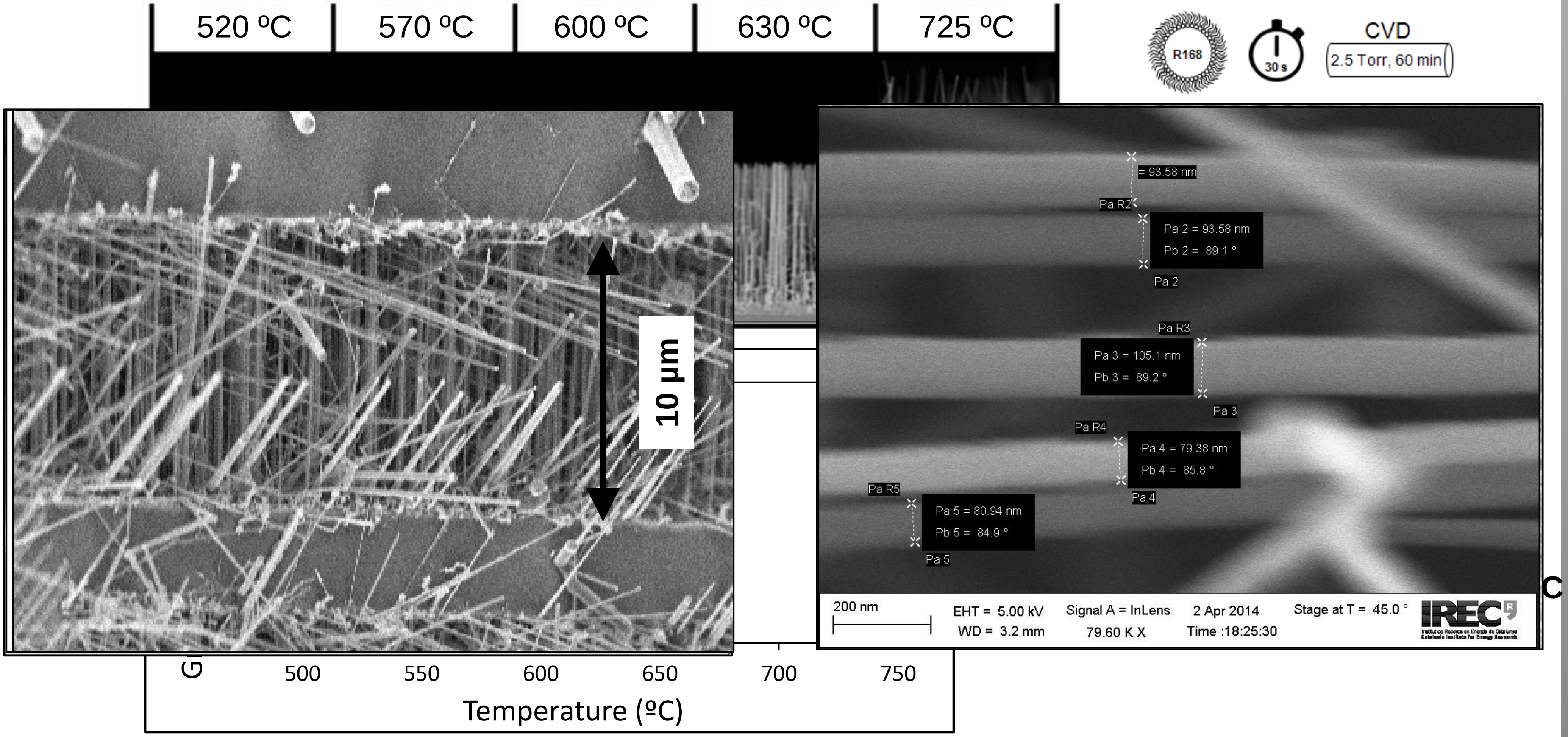
- **Growth rate increases with T**
- **Verticality has a maximum in 630 ºC**

CVD-VLS – Nanowire control – Effect of temperature



- **Well aligned horizontal Si NWs were obtained in trenches**

CVD-VLS – Nanowire control – Effect of temperature



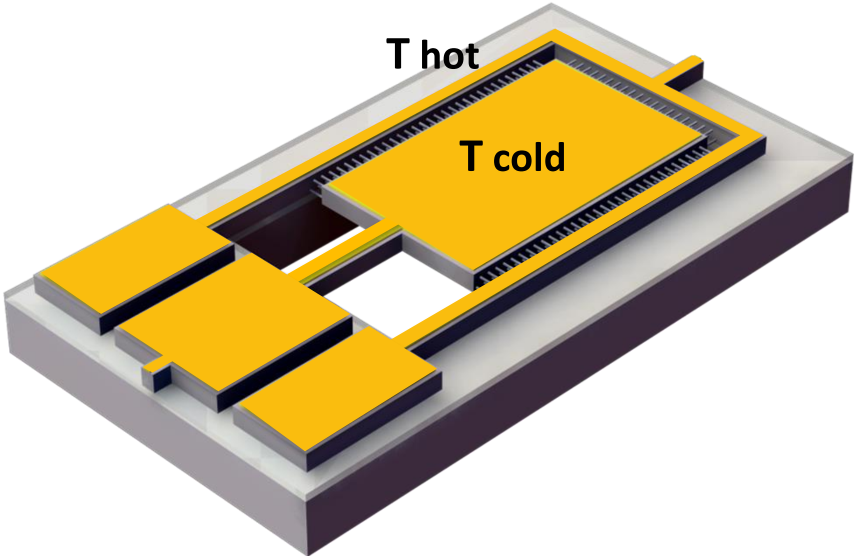
- ❖ **Well aligned horizontal Si NWs were obtained in trenches**

Bottom-up strategy – Device layout

Structural core will be a Si device micromachined in such a way that hot and cold areas develop when resting on a hot surface.

Hot area: surrounding rim **Cold area:** suspended platform.

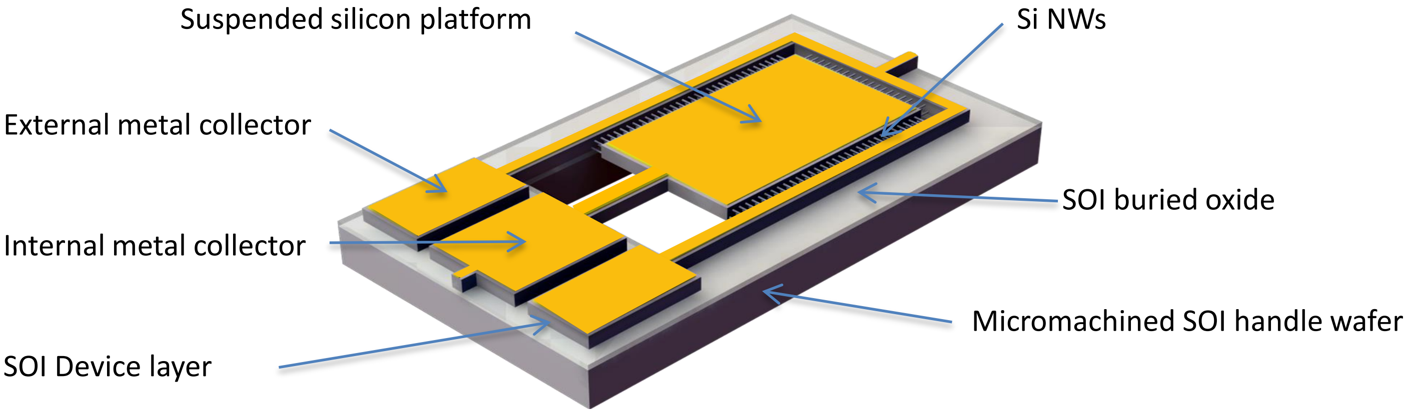
Thermocouple: nanostructured silicon and thin metal film.



European Union
European Regional Development Fund
SEVENTH FRAMEWORK PROGRAMME

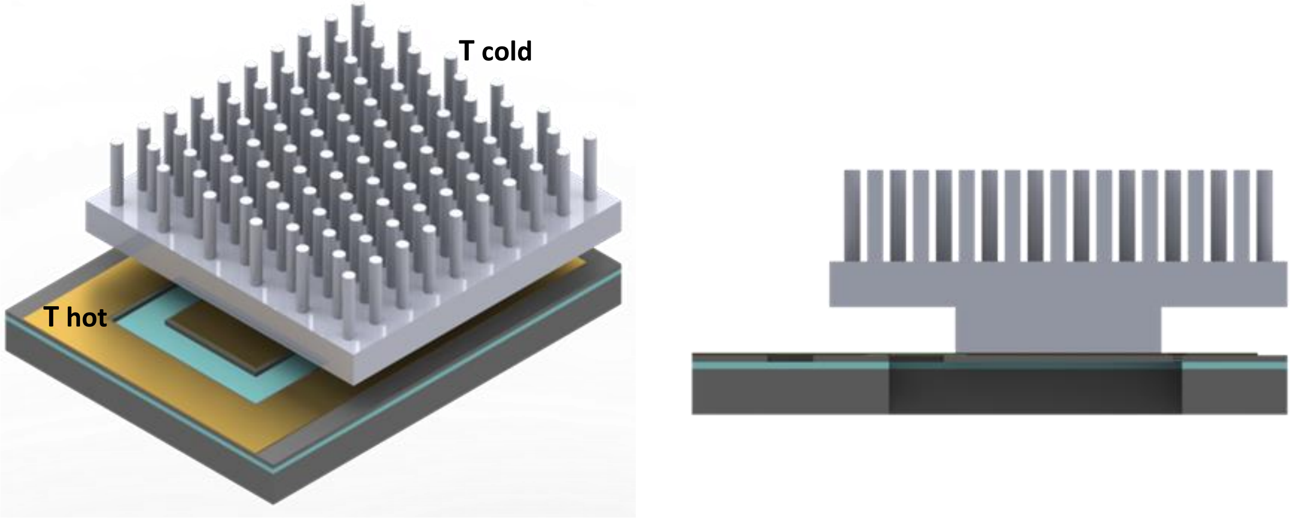
Bottom-up strategy – Device layout

- SOI wafers used as starting material. Device layer <110>, so that parallelograms with <111> oriented walls can be built .
- Typical dimension will be 1 mm, with 10 µm trench widths. Depth is fixed by device layer thickness, which will be around 10-15 µm to accommodate a large number of NWs.



Bottom-up strategy – Microradiator

- Integration of a microradiator in the cold side to efficiently convey into the active area the vertical thermal gradient present in the application scenario.
- Overhanging thermal conductive structure (metal/silicon) supported by a pillar in close contact with cold platform.

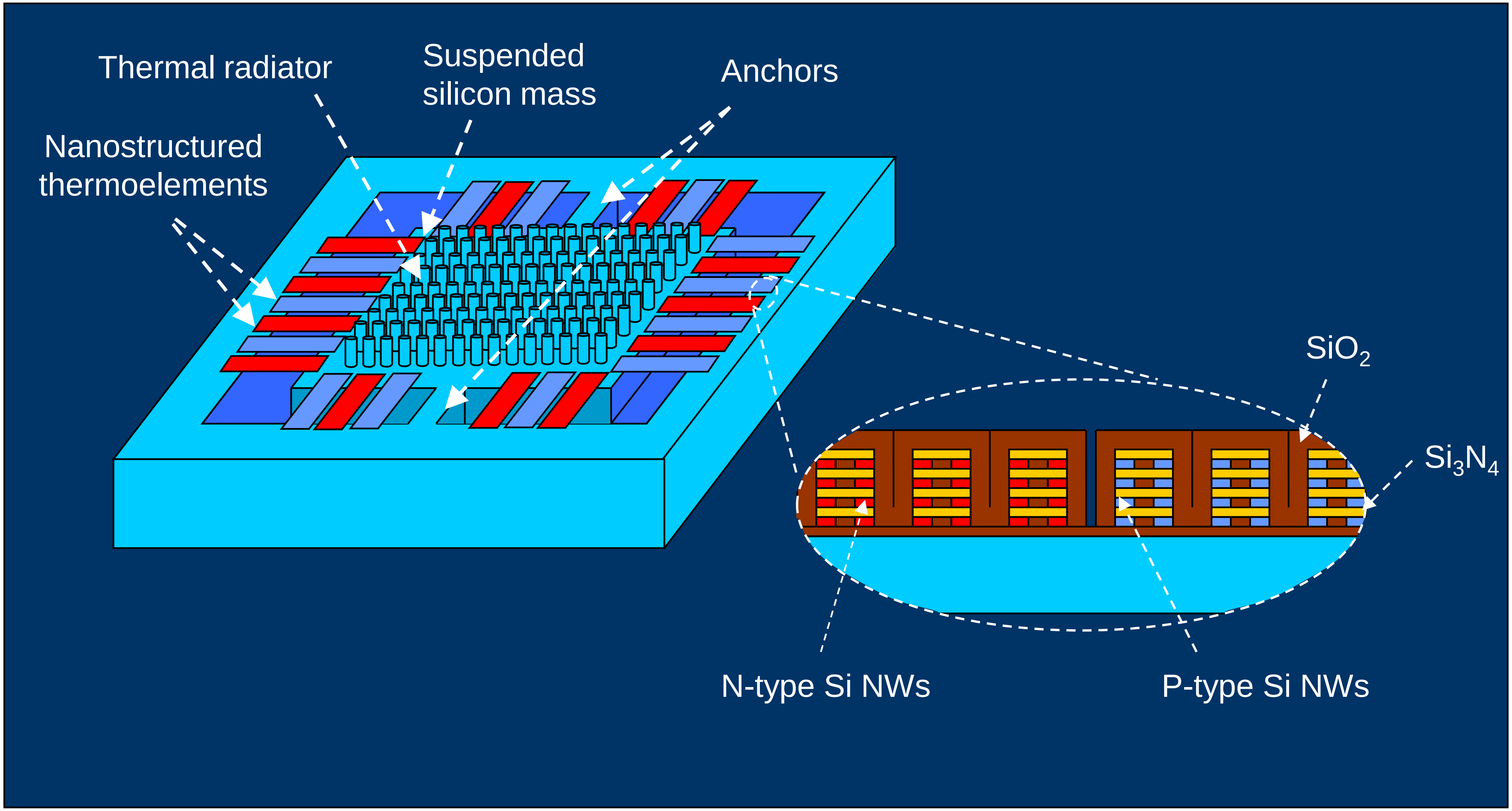


Top-down strategy – Device layout

NWs will be grown with a CVD method within nanometric cavities built up by controlled etching and filling of recessed regions (without nanolithographic steps).

Semicond. Sci. Technol. 26 (2011) 045005

Top-down layout with lateral NWs:



Top-down fabrication of lateral NWs:

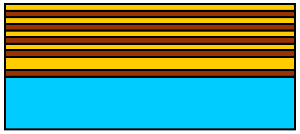
1. Si substrate

2. SiO_2 growth

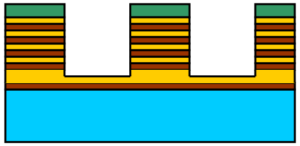
3. Si_3N_4 deposition

4. SiO_2 deposition

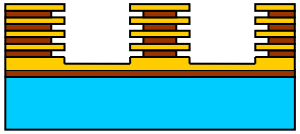
5. Si_3N_4/SiO_2 deposition



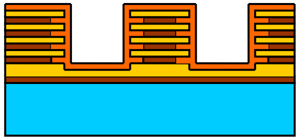
6. Si_3N_4/SiO_2 RIE



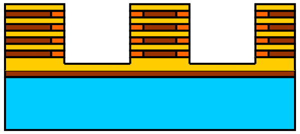
7. SiO_2 wet etching



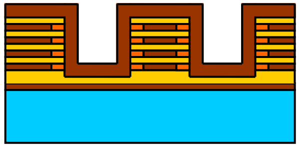
8. Poly deposition



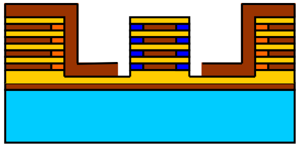
9. Poly etchback



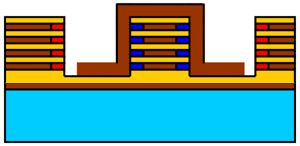
10. SiO_2 deposition



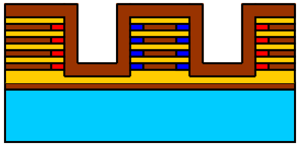
11. P-type doping



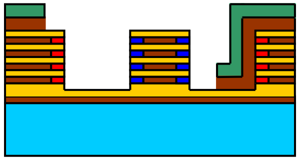
12. N-type doping



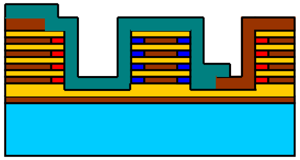
13. SiO_2 deposition

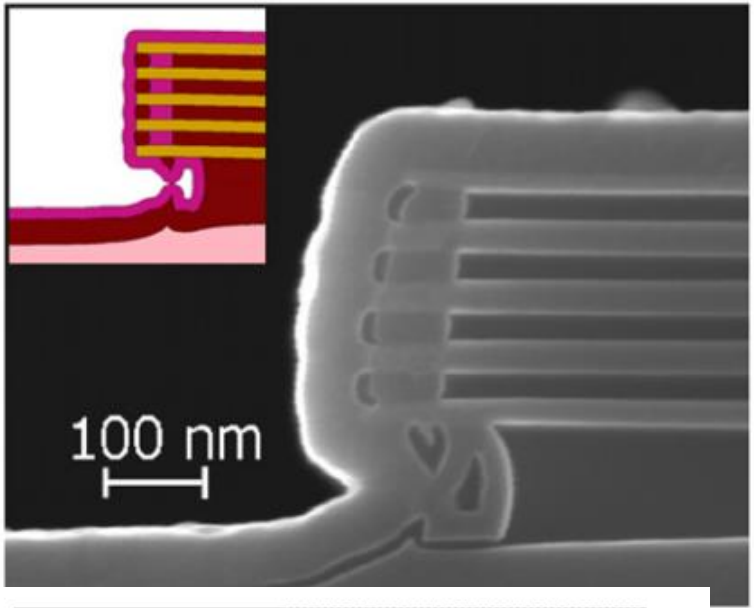


14. SiO_2 etching



15. Al patterning





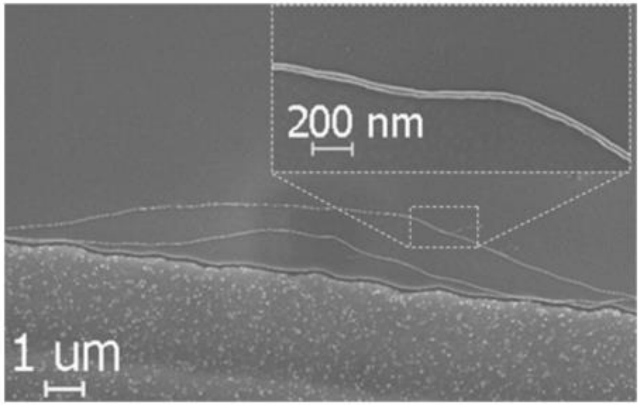
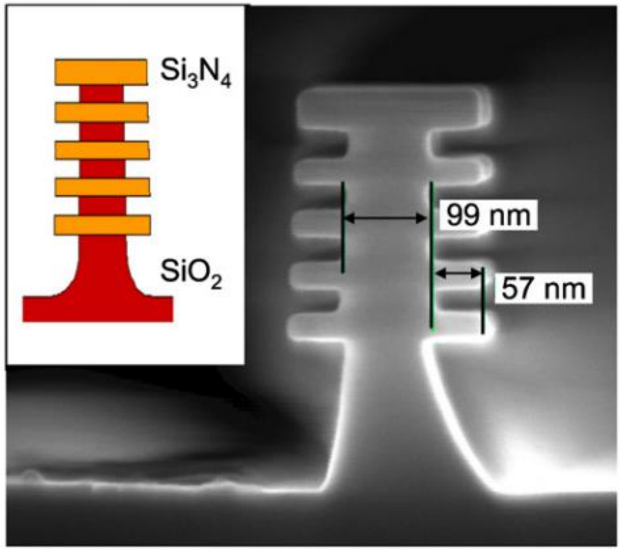
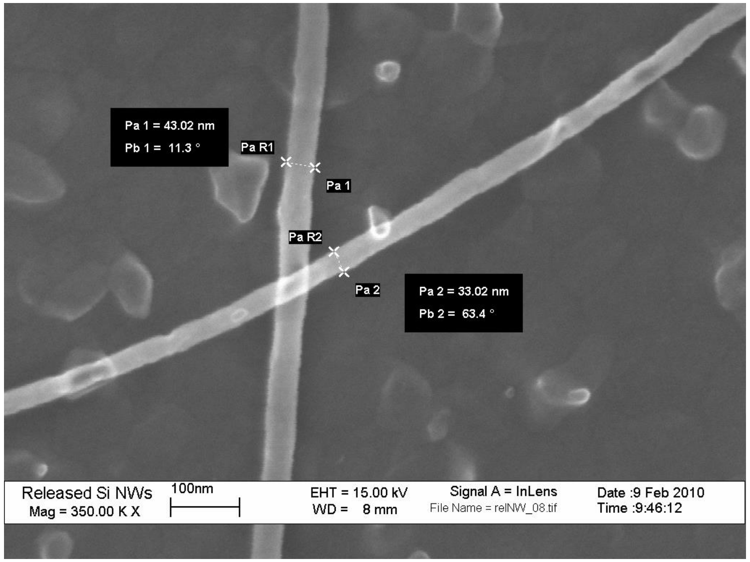
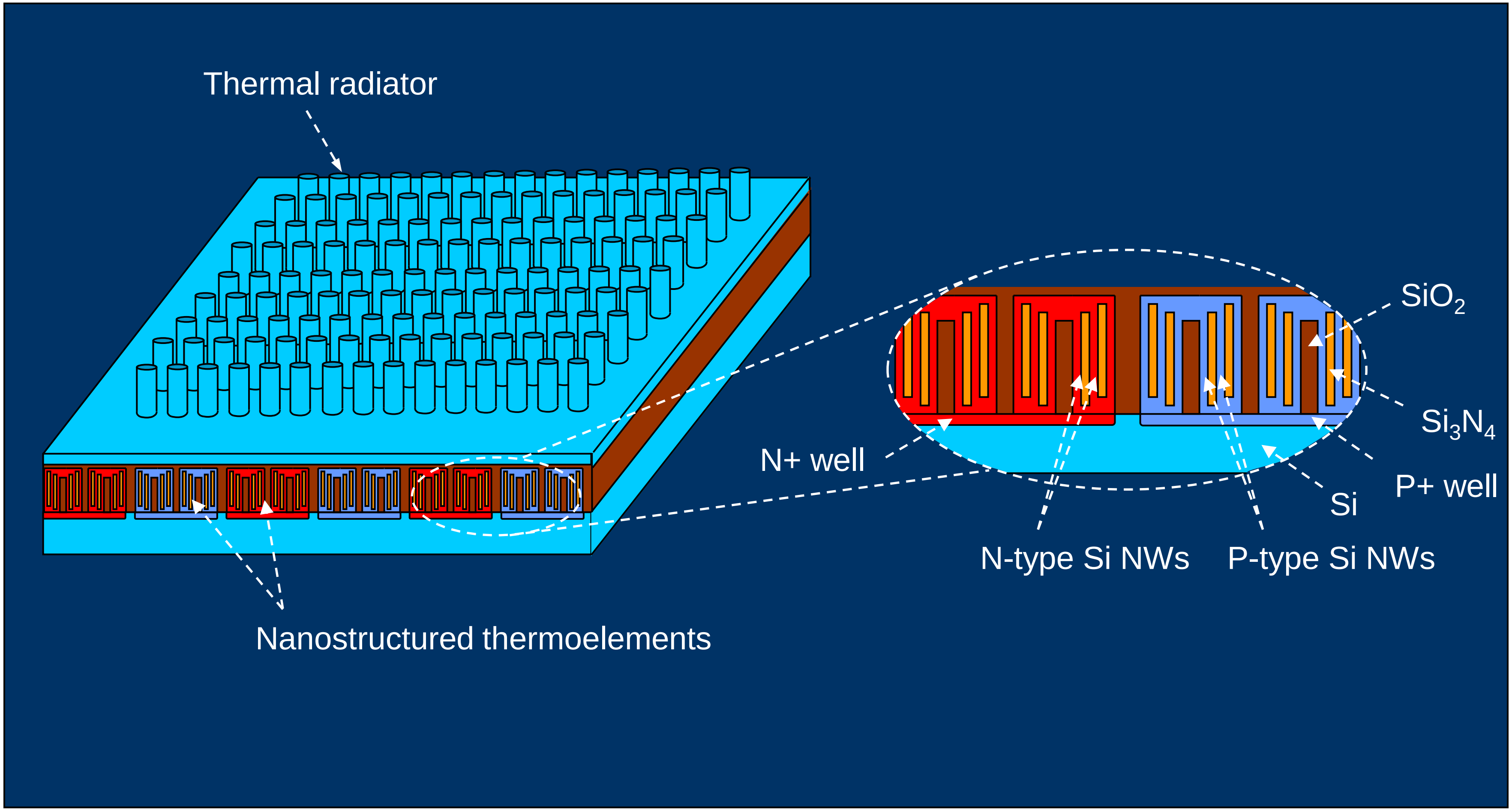


Fig. 5. SEM images at different magnifications of the nanowire after detachment from the hosting structure.





Top-down layout with vertical NWs:



From aims to practice

- NWs have high R_{th} ($\approx 10^{6}$ K $W^{-1}nm^{-1}$ /NW)
- For $\Delta T = 50$ K, max heat acceptance is ≈ 25 pW/NW @ wire length of 1 mm
- If $\eta = 5$ % a target power output of 10 µW/cm^{2} requires a wire density of 10^{8} cm^{-2}, i.e. a wire spacing of about 1 µm

From aims to practice

Critical design issues are:

- optimal wire length
- optimal geometry (lateral or vertical)

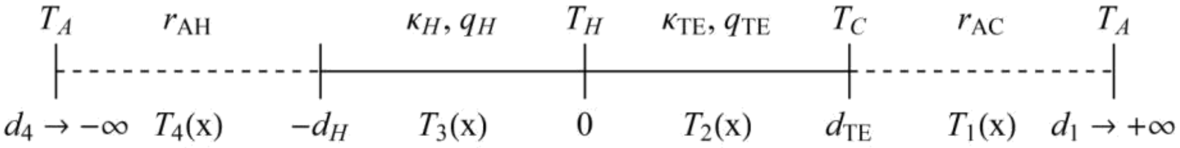
TEG modeling

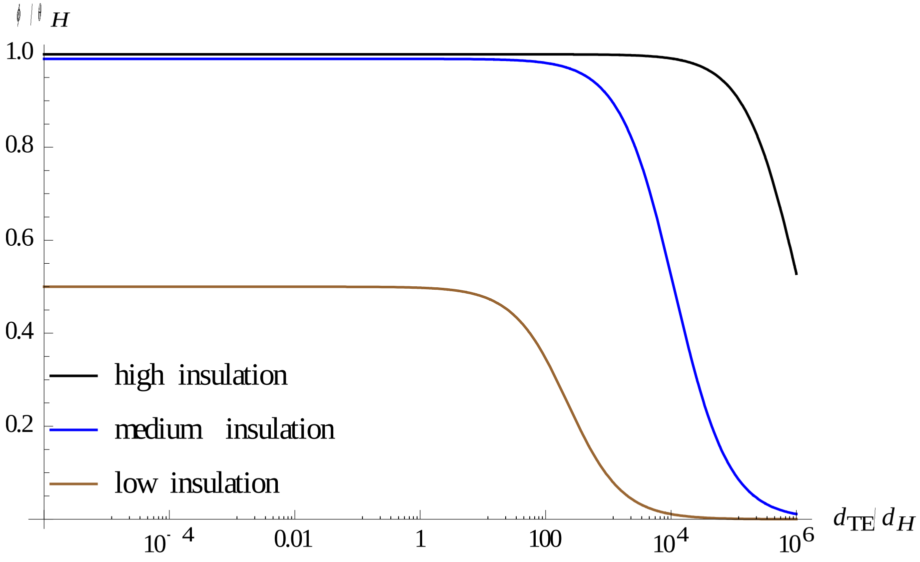
Choice of boundary conditions leads to contrasting design indications:

$$W_{\mathrm{el}} = W_{\mathrm{th}}\eta_{\mathrm{TE}} = (\Delta T/R_{\mathrm{th}})\eta_{\mathrm{TE}}$$

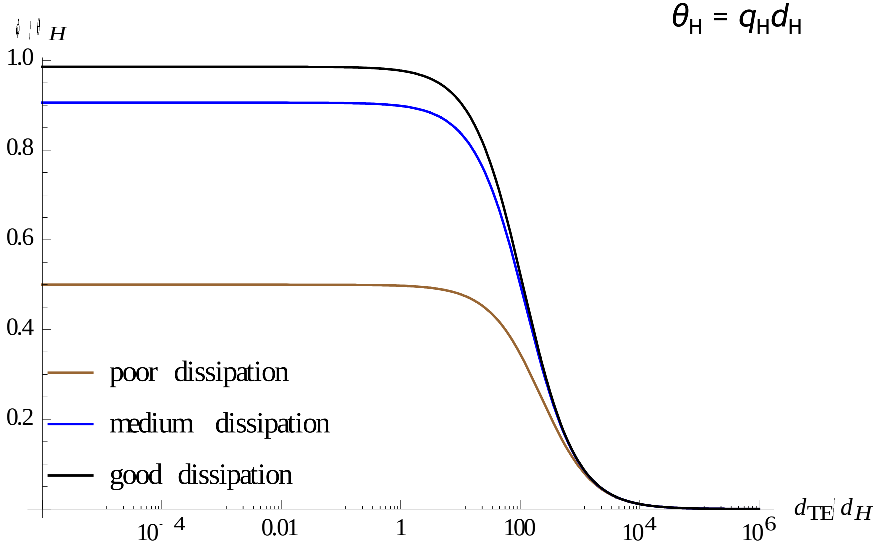
- setting fixed-T b.c.s: W_{el} increases as R_{th} decreases
- setting fixed-heatflow b.c.s: W_{el} increases as R_{th} increases

TEG modeling

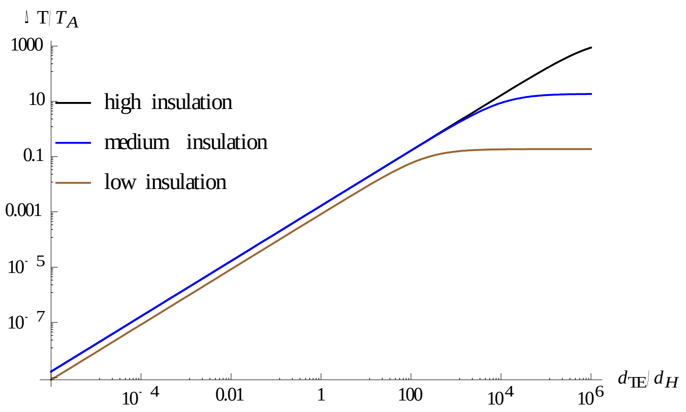


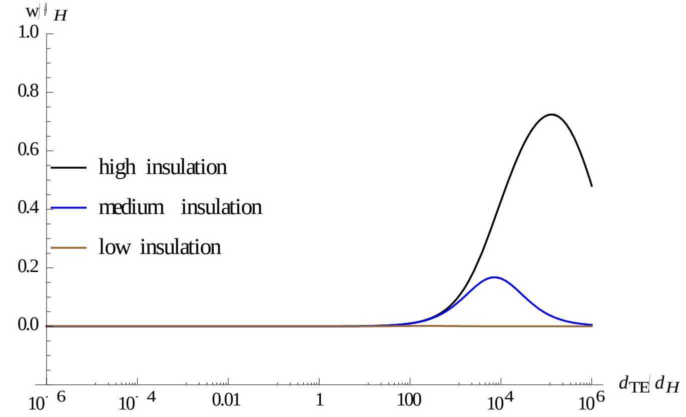


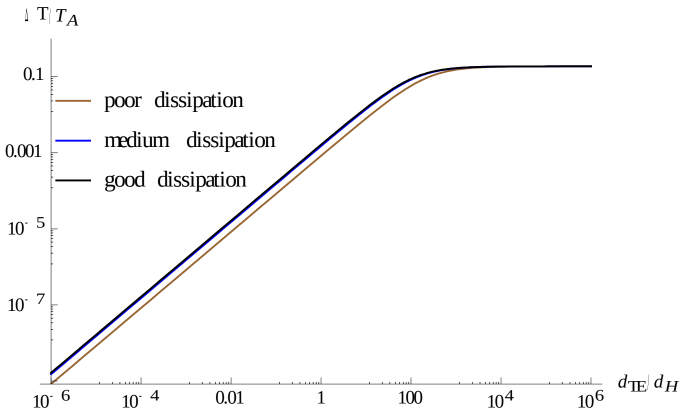
$\theta_H = q_H d_H$

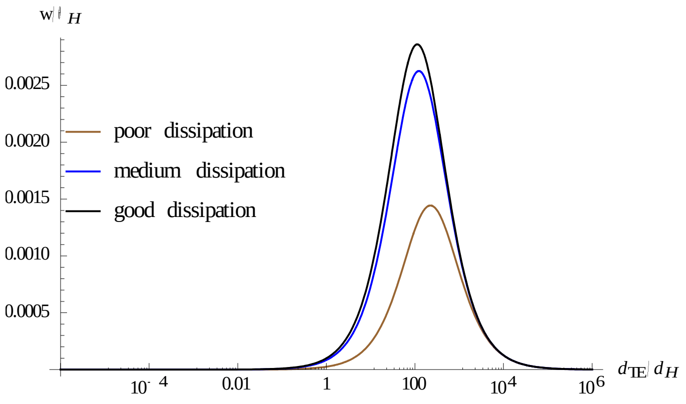


TEG modeling

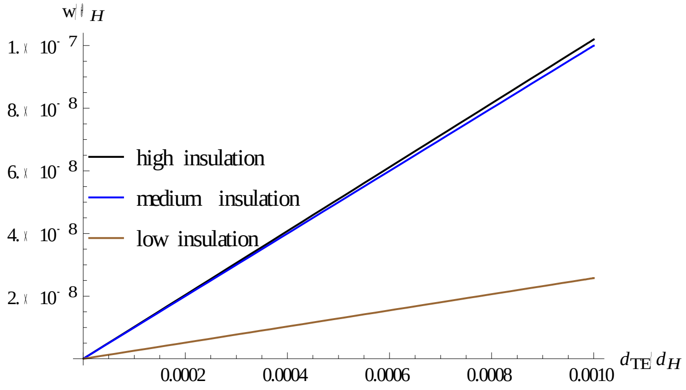


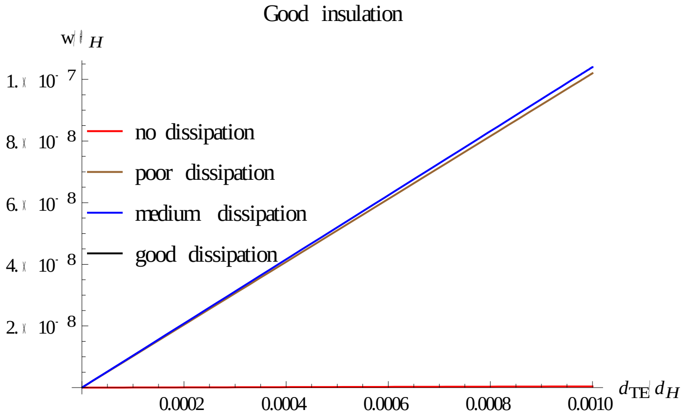


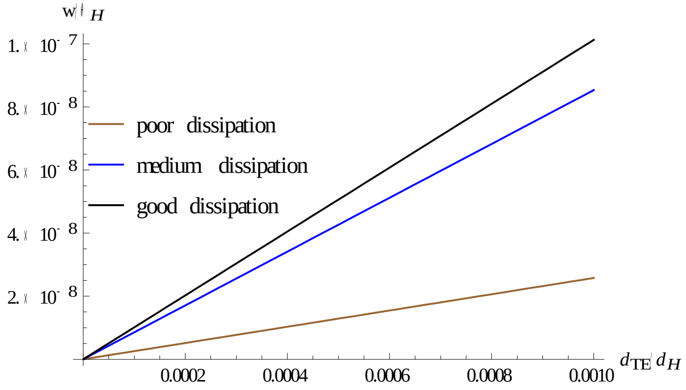




TEG modeling







Thus:

- longer nanowires raise power output
- effective dissipation is relevant for poorly insulated heat sources

Heat administration

TEGs will be mounted into a proper package that will deliver heat:

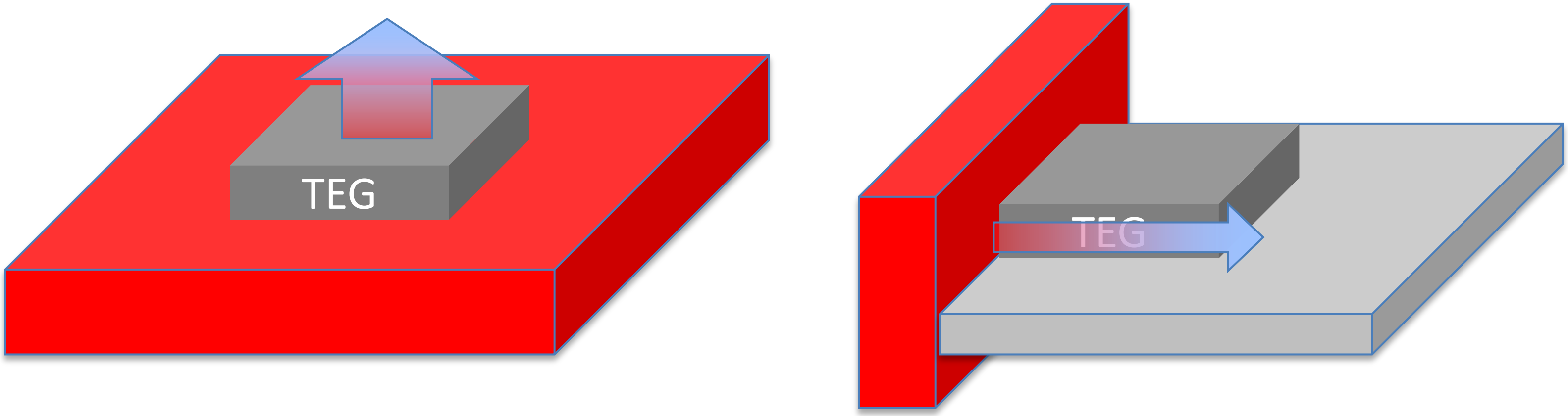
heat source → TEG → cold sink → ambient

- Higher heat radiator efficiency if series thermal resistances are small
- Parallel (shunt) resistance must be minimized

Both requirements are better satisfied if TEG geometry simplifies package design

Heat direction

Two geometries (three layouts) addressed as of the 1st TEG generation



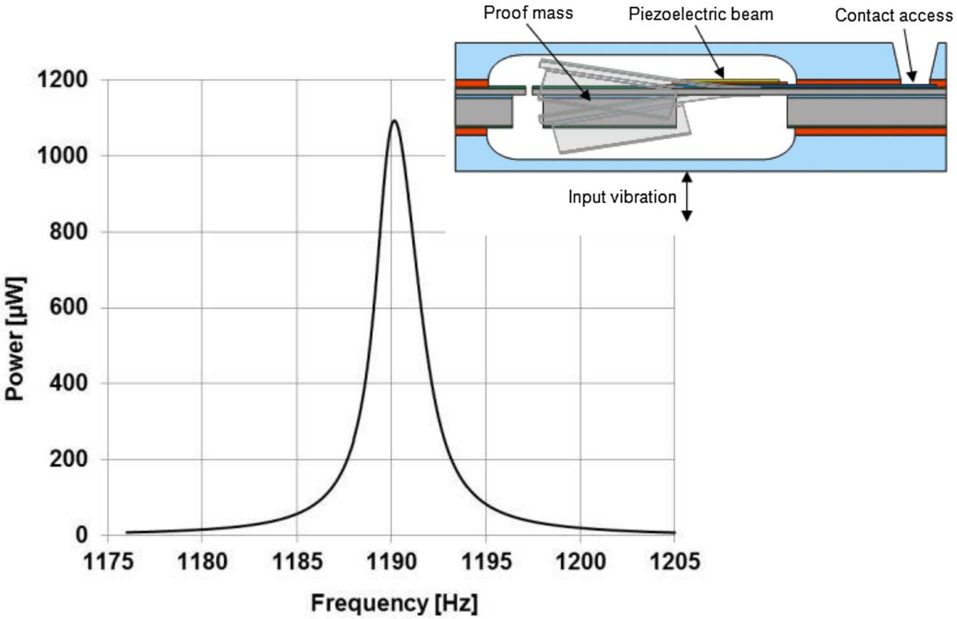
Mechanical harvesters

Tire pressure monitoring system (TPMS)

- Today
  - – Battery powered
  - – Rim or valve mounted
- Battery replacement costs and effort
  - – Energy harvester + system on the tire
    - Tire temperature
    - Tire identification

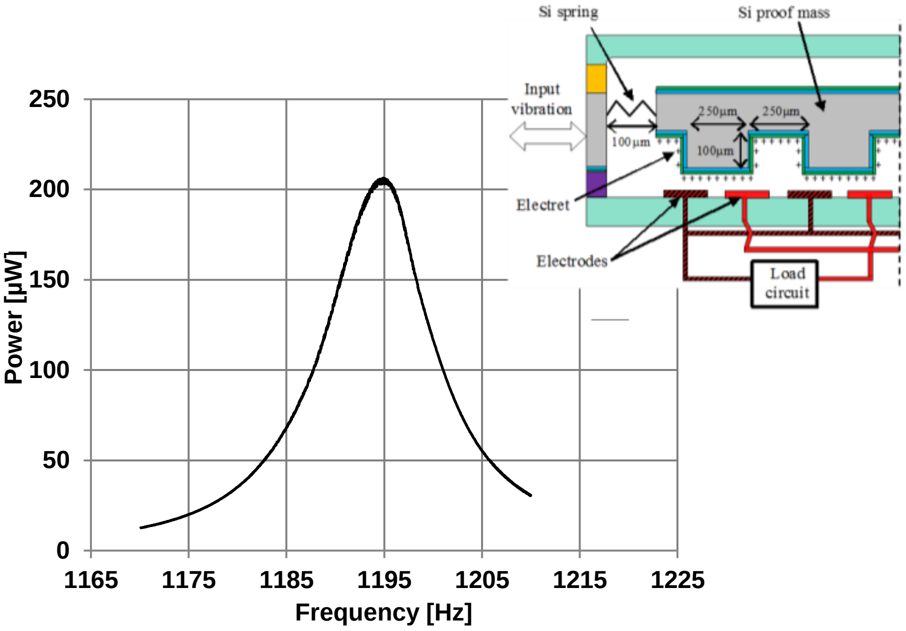
Sinusoidal excitation

Piezo



- Power output of 1100µW
- Quality factor Q : 530
- Bandwidth BW : 2.3Hz
- Sensitivity : 262 µW/g^2

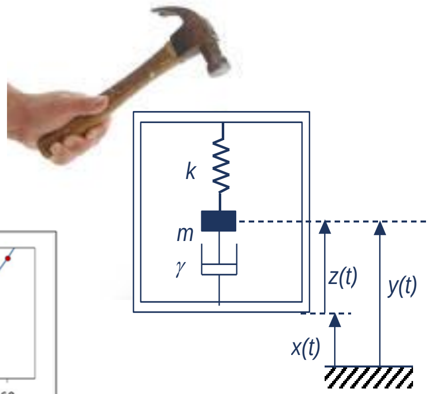
Electrostatic



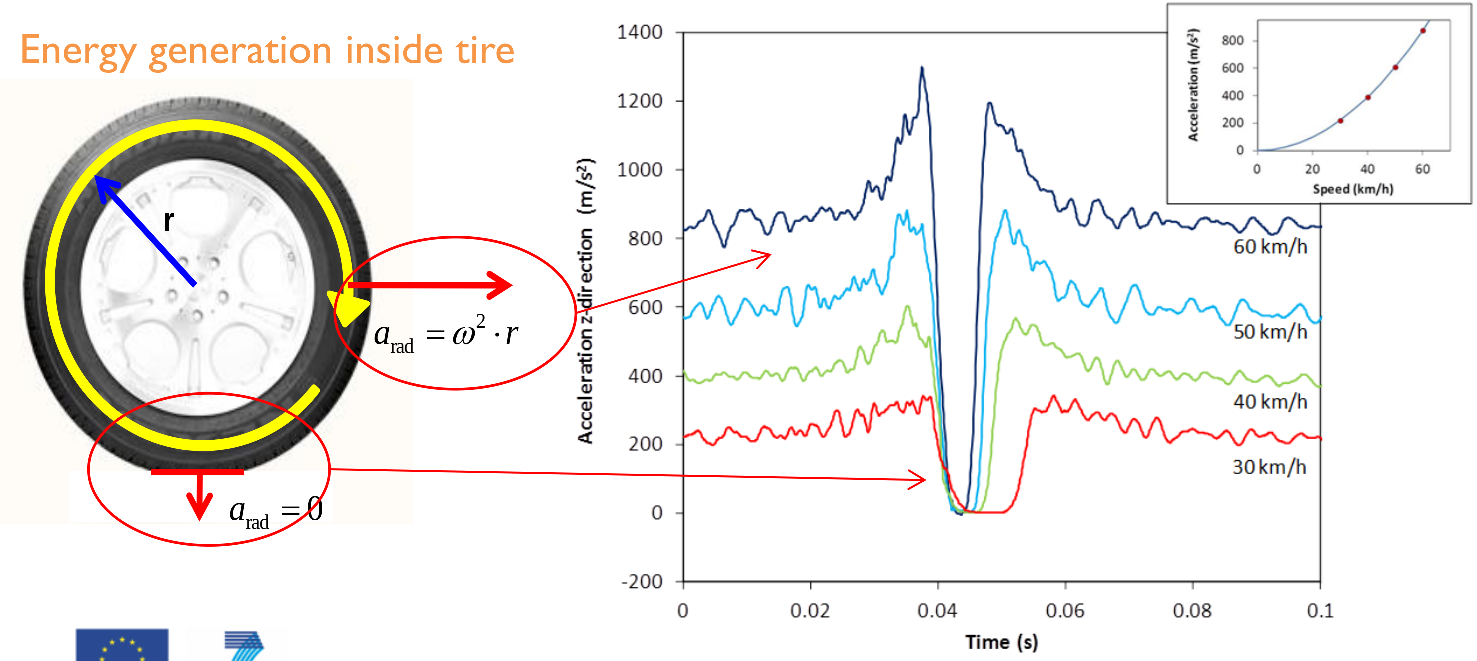
- Power output ~ 200µW
- Quality factor Q : 93
- Bandwidth BW : 12.8 Hz
- Sensitivity : 130 µW/g^2

- Shock excitation inside tire
  - Power generation by shock excitation
  - Large shock available inside tire
  - Up to 100µW @ 100km/h is feasible

Velocity damped resonator

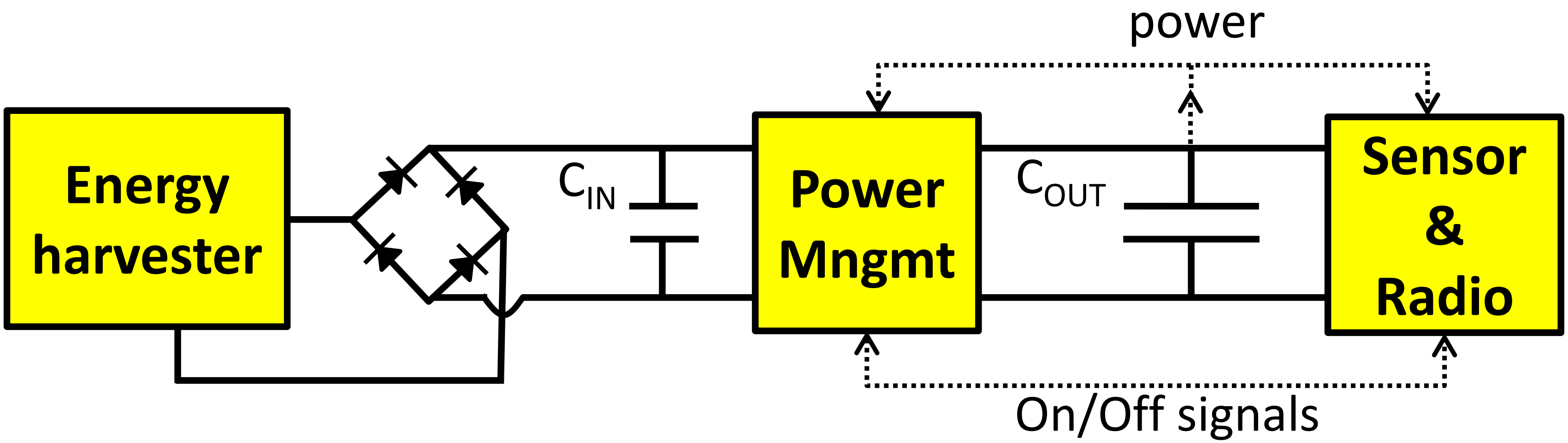


Energy generation inside tire



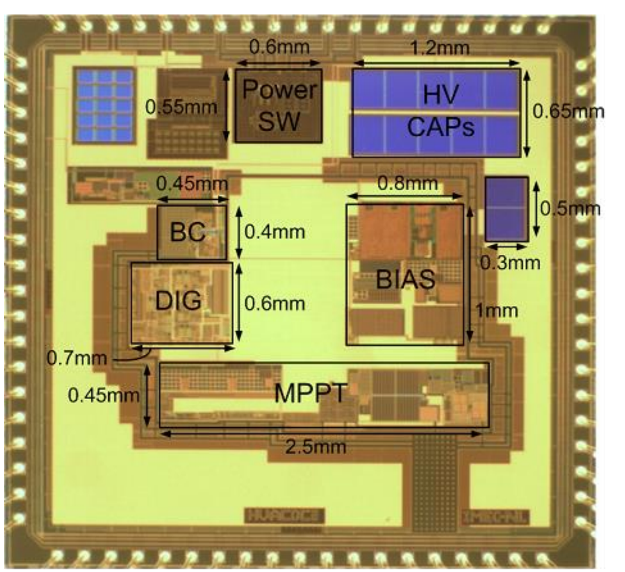
Power generation is discontinuous

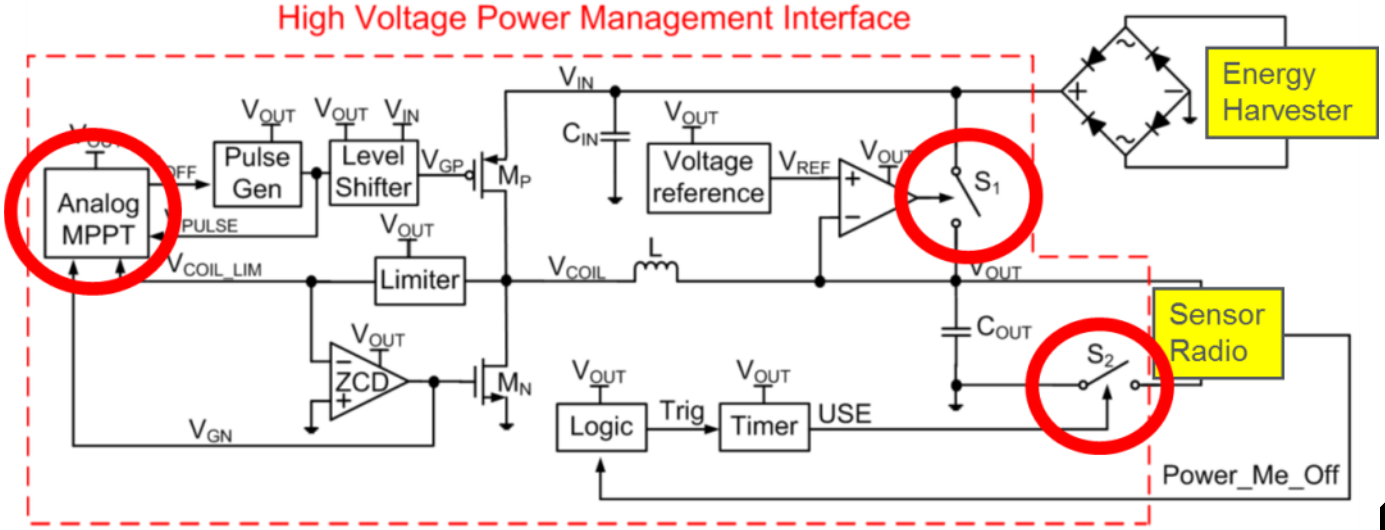
- Schematic system architecture



SiNERGY

- Power Management
  - High voltage
  - 2 switches
  - Maximum Power Point Tracking
  - start-up from zero
  - η=88% at low power
  - V_{out}~ 2.5 V_{DC}





European Union

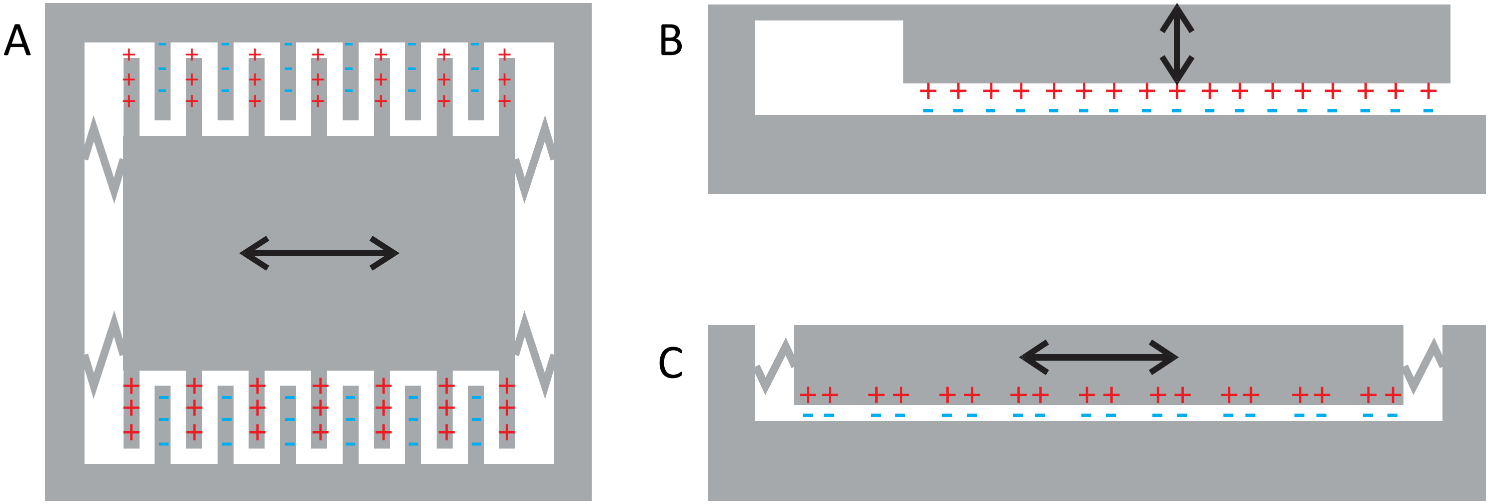
SEVENTH FRAMEWORK PROGRAMME

Electrostatic energy harvesters

What do we need?

- Vibrating mass
  - Mass
  - Flexible springs
- Variable capacitor
  - Polarization source - charged electret
  - Electrodes
- Packaging
  - Capping

- Different operation principles possible

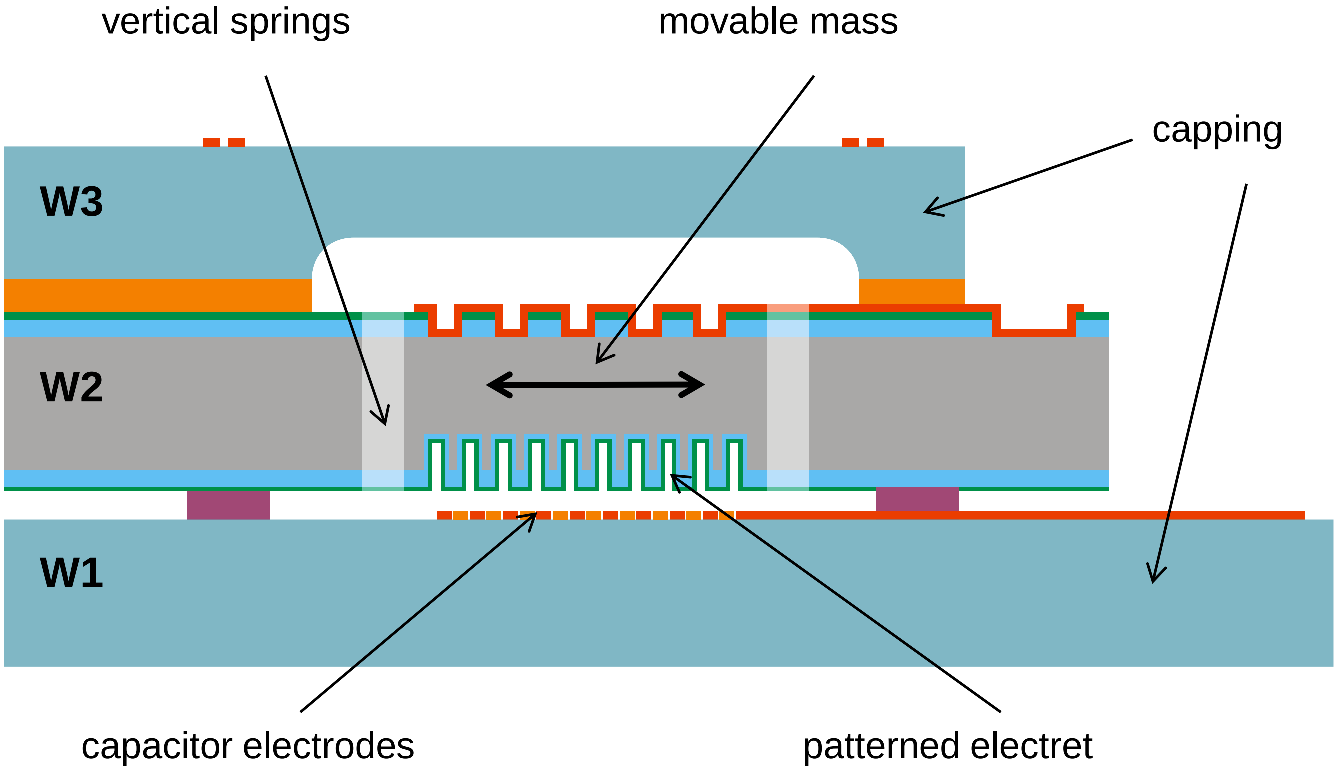


A) in-plane gap closing

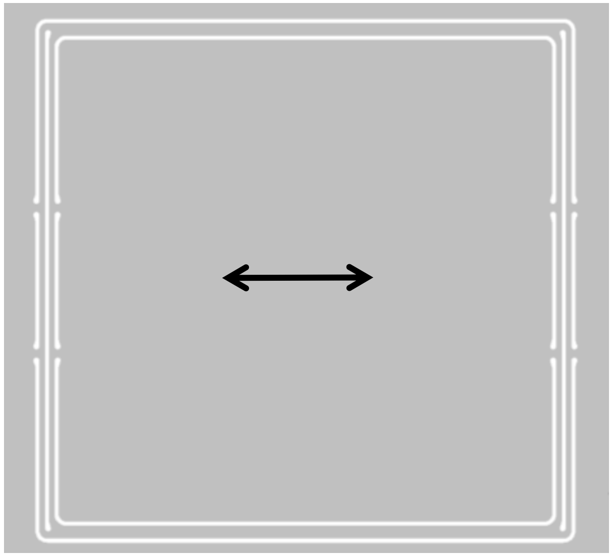
B) Out-of-plane gap closing

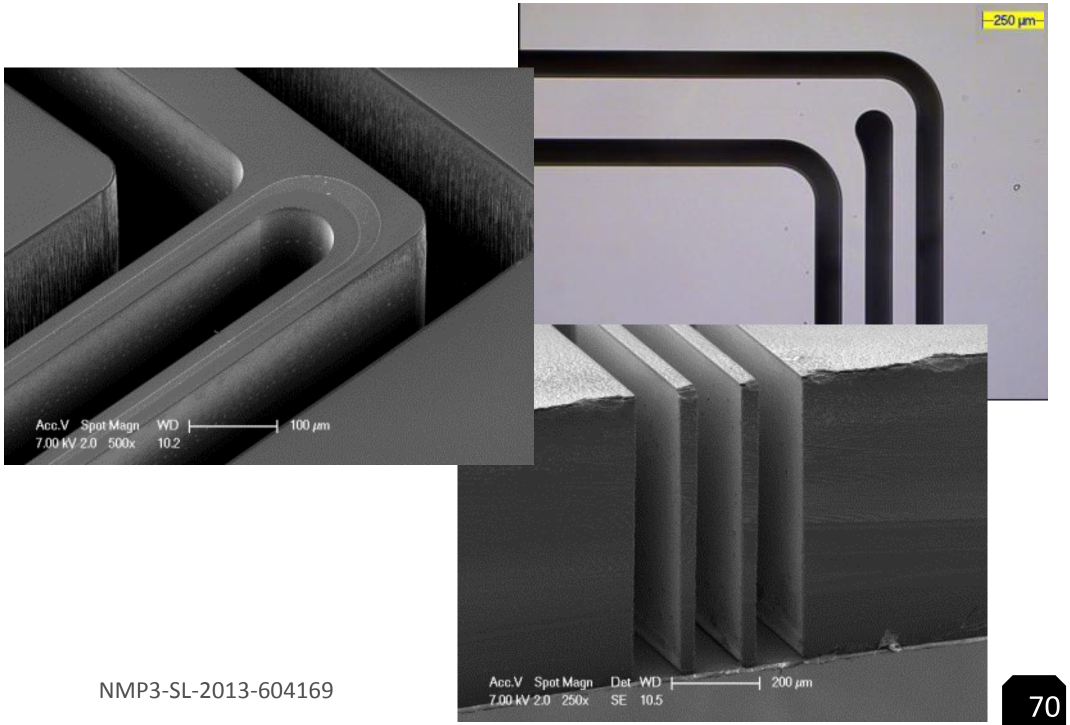
C) In-plane sliding capacitor

- In-plane sliding capacitor



- Device layout – mass/springs system
  - 1 cm^2 mass, full wafer thickness (650 µm)
  - 80µm thin springs, full wafer height
  - 100µm etched trenches, 100µm max mass amplitude



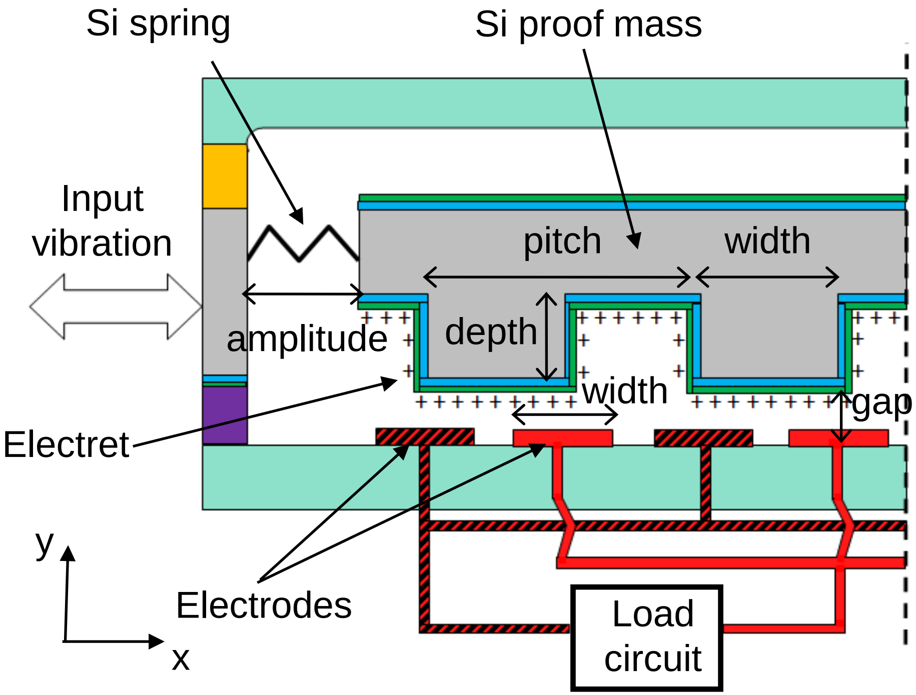


- Materials – Electret
  - Polymers (PVDF, BCB, Cytop) - low temperature stability
  - Inorganic materials (SiO_2, Si_3N_4) - CMOS compatible deposition

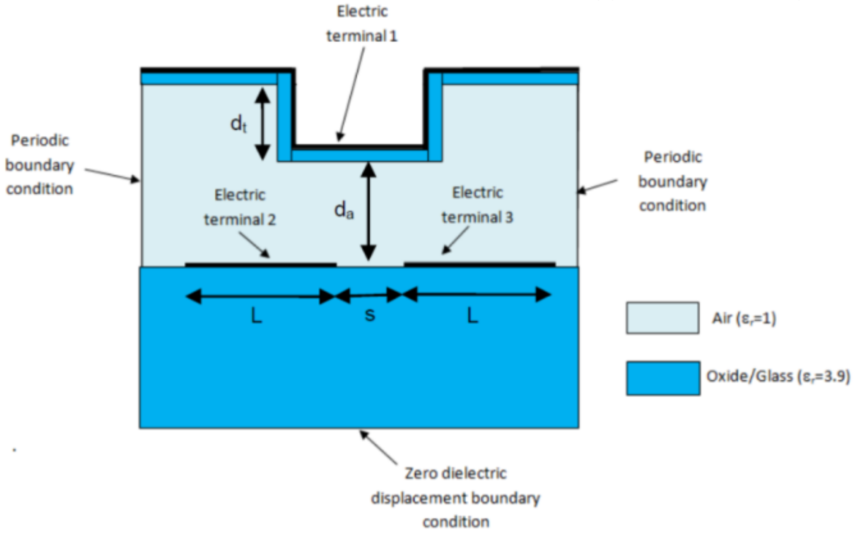
- Interface SiO_2-Si_3N_4 can trap stable charges
- Parameters to play with:
  - Oxide Thickness
  - Nitride Thickness
  - Material quality (deposition method)
  - Multilayers
  - Charge patterning method

- Electret layer – results and choices
- SiO_2 thickness:
  - 500nm - charge decay
  - 2000nm - no charge separation after RTA
  - 1000nm - good
- Si_3N_4 thickness:
  - Little influence, 150nm - good
- Deposition method:
  - Thermal oxide + LPCVD Si_3N_4 - good
  - TEOS, PECVD oxide and nitride - charge decay
- Multilayers: no extra charge

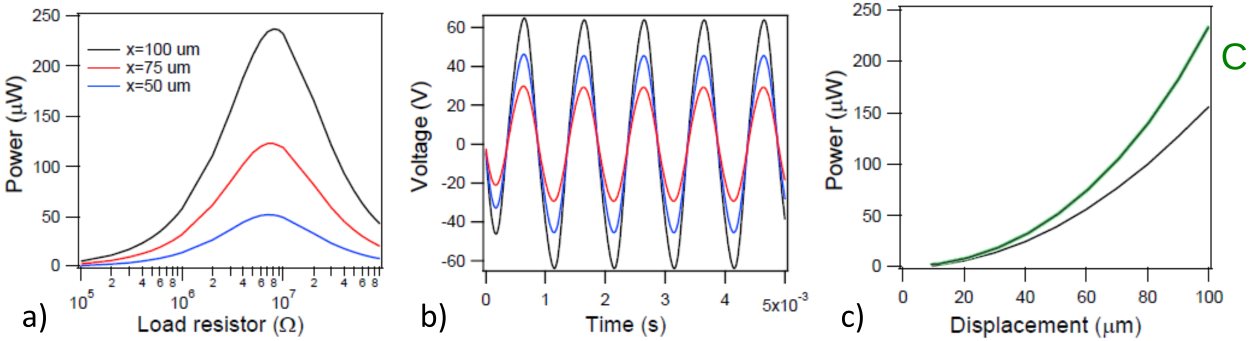
- Device layout – electret / electrode configuration



- Device layout – optimization
  - Finite element modelling



- Typical modelling result



Corrugated electret

vs

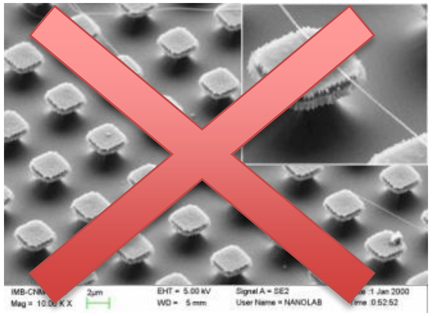
Planar electret

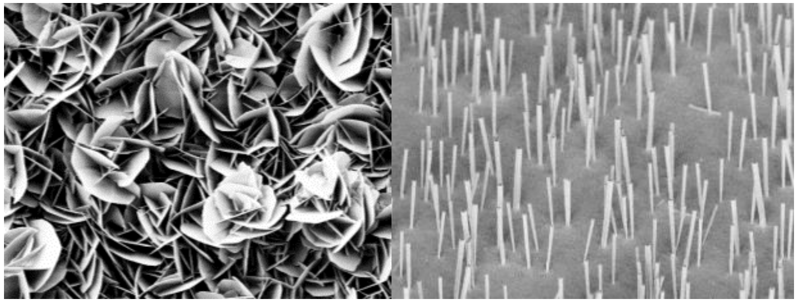
- Predicted maximum output power: 500µW
  - 1kHz 2.5G sinusoidal input vibration (resonance), full 100µm mass displacement

Piezoelectric harvesting

New approach uses ZnO nanowires (NWs) and nanosheets (NSs)

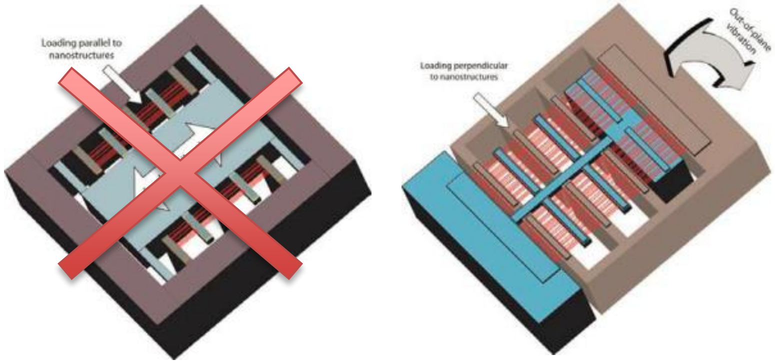
Standard AlN thin-film approach will be used as a benchmark

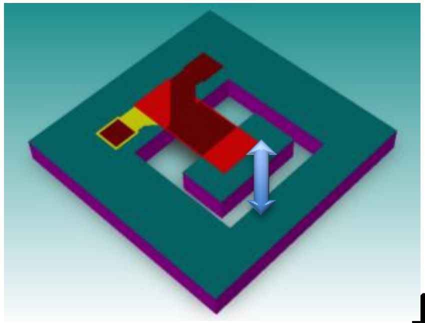




ZnO nanowires are much easier to grow and integrate with silicon

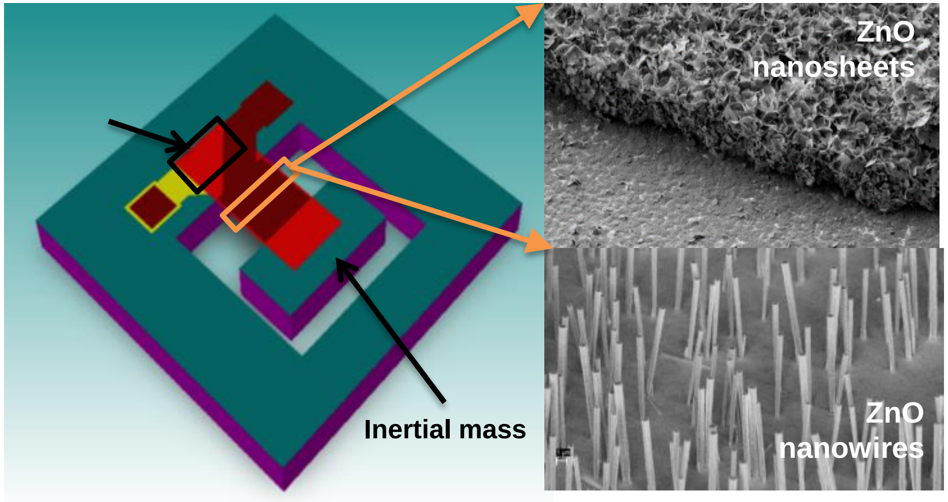
ZnO NW & NS growth is also a low-cost solution and a hot-topic



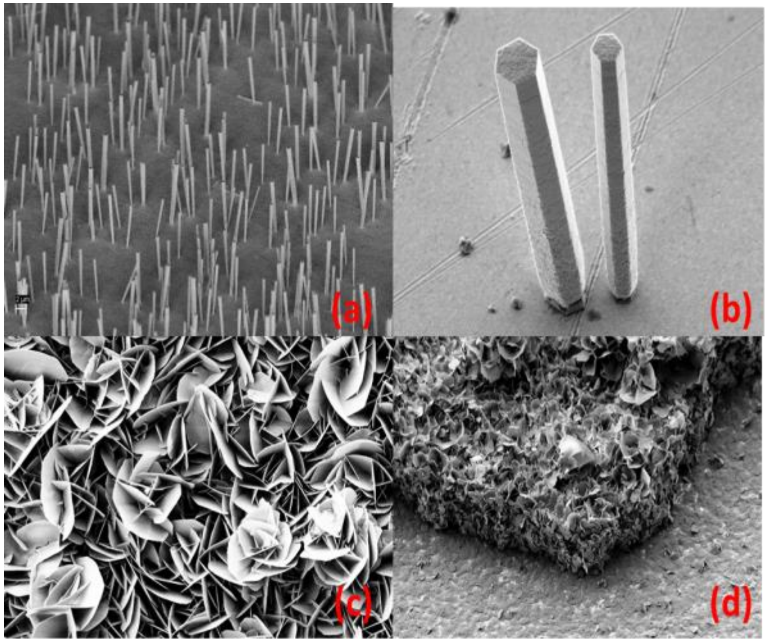


What do we need?

- Inertial mass & cantilevered spring
  - Mass
  - Flexible spring
- Piezoelectric material
  - ZnO nanowires & nanosheets
  - AlN thin-film (for benchmark)
  - Electrodes

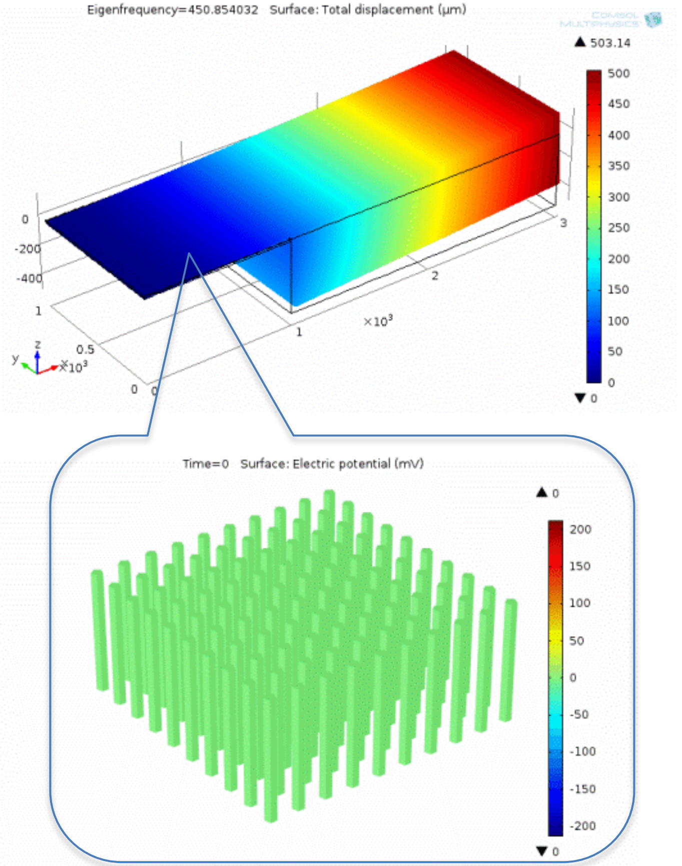


- New piezoelectric materials
  - ZnO nanostructures will be used as **replacement of original approach** based on nanofibres:
    - ZnO nanowires .
    - ZnO nanosheets .
  - More mature technology compared to nanofibres that needs a more important technology development
  - **Inherent piezoelectric behavior of ZnO**
  - Easier to integrate with silicon
  - **High novelty provided by ZnO nanosheets**



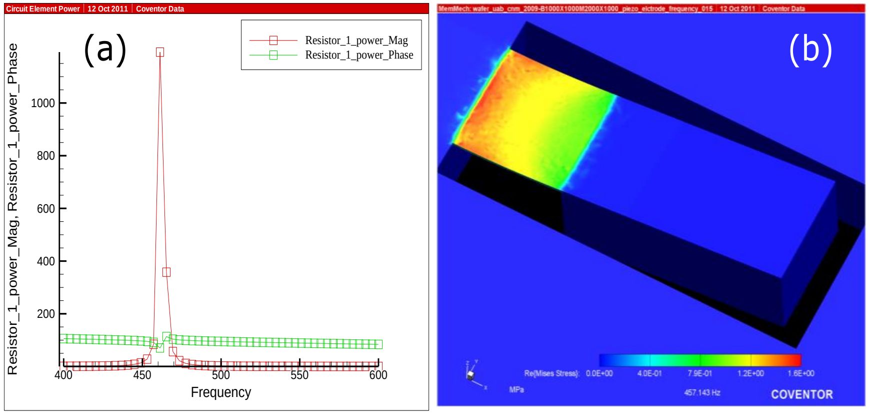
ZnO nanowires (overall view (a) and detailed view (b)), and nanosheets (top view (c) and tilted view (d)). NW lengths rate from 2 to 5 µm and thicknesses from 100 nm to 900 nm.

Predicted output power



For FEM simulations a **power density of 47 µW/cm^2** at 447 Hz (Q = 50) for 1 g has been calculated.

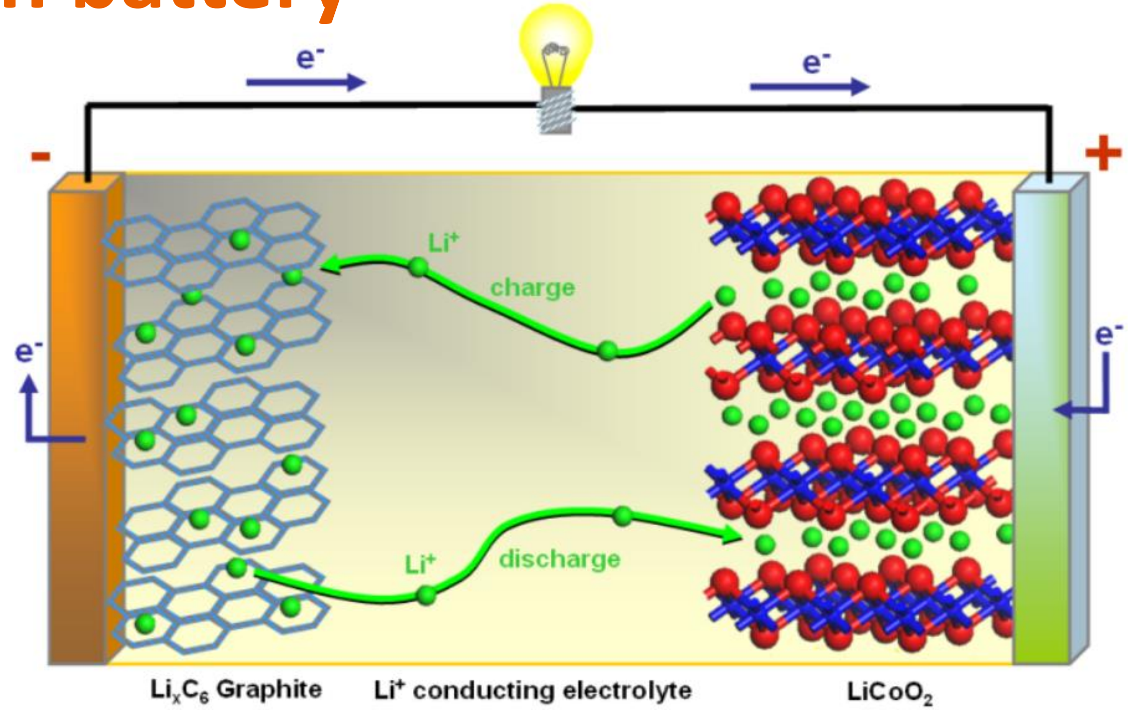
An expected power density of around **400 µW/cm^2** for an acceleration of 10 g is a **good target.**



Generated power (in nW) and main stress in the structure when it is bent

Batteries

Li-ion battery

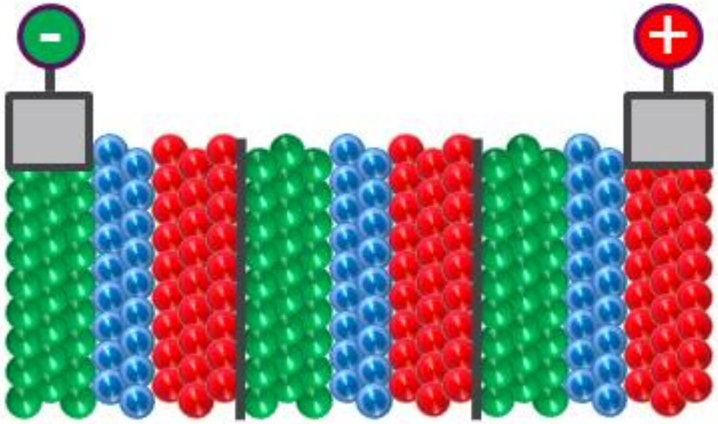


Charge and discharge process of an Li-ion battery

During charging Li$^+$ ions are liberated from the cathode and transported through the liquid electrolyte to the anode, where the Li$^+$ is reduced by the electrons coming from the electrical circuit.

THICK BATTERIES

kWh - Wh

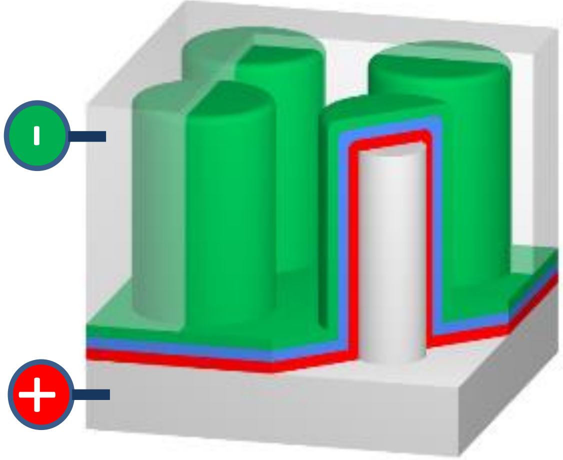


High capacity devices with competitive power

- *Pressed pellets/bipolar stacks*
- *Solid electrolytes with high σ_{ionic}*
- *Low-impedance interfaces*

THIN-FILM BATTERIES

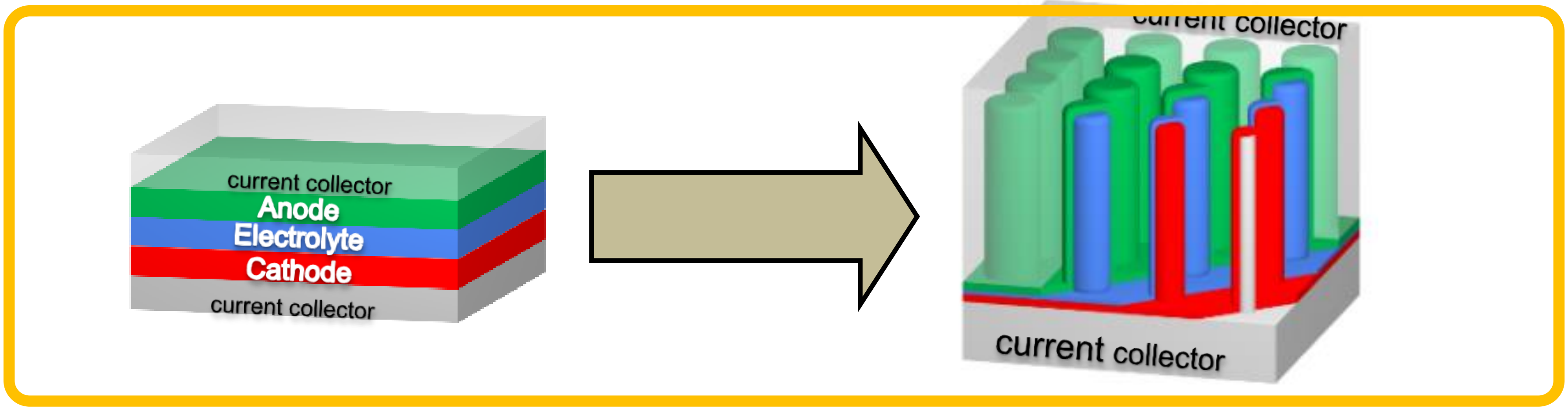
Wh - mWh



High-power devices with competitive capacity

- *Film thickness scaling*
- *3D surface area enhancement*
- *Process up-scaling/large area foils*

Fabrication of functional thin-film micro-battery for integrated storage



Planar thin-film device

Lattice matched spinel stack

Electrolyte and interface engineering for power (charging rate)

0.05 mAh/cm^2 at 0.1C, and 60% capacity at 10C (1 mA/cm^2)

3D thin-film battery

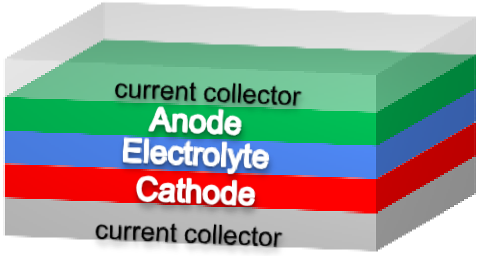
Si compatible fabrication process

Micro-structured architectures for increased battery capacity and power (current)

0.5mAh/cm^2 at 0.1C, and 50% capacity at 5C rate (2.5 mA/cm^2)

Standard planar micro-battery integration

One **interface** ***at a time*** **approach**



Current collector

TiN, Pt, SiC, TiC, Cu

$Li_4Ti_5O_{12}$ **Anode** (1.55V vs. Li^+/Li)

- *Negligible volume expansion*
- *Spinel structure*
- *Capacity: 610mAh/cm^3*

$Li_4Ti_5O_{12}$
TiO_2
a-Si

Solid State Electrolyte Requirements

1. *Pinhole-free*
2. *High ionic conductance ($\sigma_i > 10^{-1}S$)*
3. *Electrochemical window (0.5 < V vs. Li^+/Li < 4.5)*
4. *Chemical stability (electrodes, Li)*
5. *Small electronic conductivity ($\sigma_e < 10^{-10}$ S/cm)*

$LiAlO_2$
Li_4SiO_4
$Li_5AlSi_2O_3$
$LiMgTiO_3$
$LiTaO_3$
$Li_xMg_{1-2x}Al_{2+x}O_4$
$Li_{3x}La_{(2/3)}\square_{x(1/3)-2x}TiO_3$

$LiMn_2O_4$ **Cathode** (4.0V vs. Li^+/Li)

- *low cost, low toxicity and abundant*
- *Spinel structure*
- *Capacity: 650mAh/cm^3*

$LiMn_2O_4$
MnO_2

Current collector

TiN, Pt, SiC, TiC, Al

Compatible material stack: Diffusion barrier, seed, CMOS processes, thermal budget compatibility

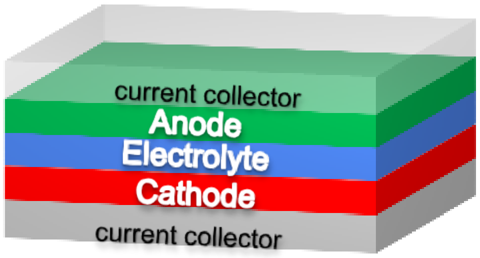
Feasibility of post-deposition **lithiation** schemes of CMOS compatible stacks

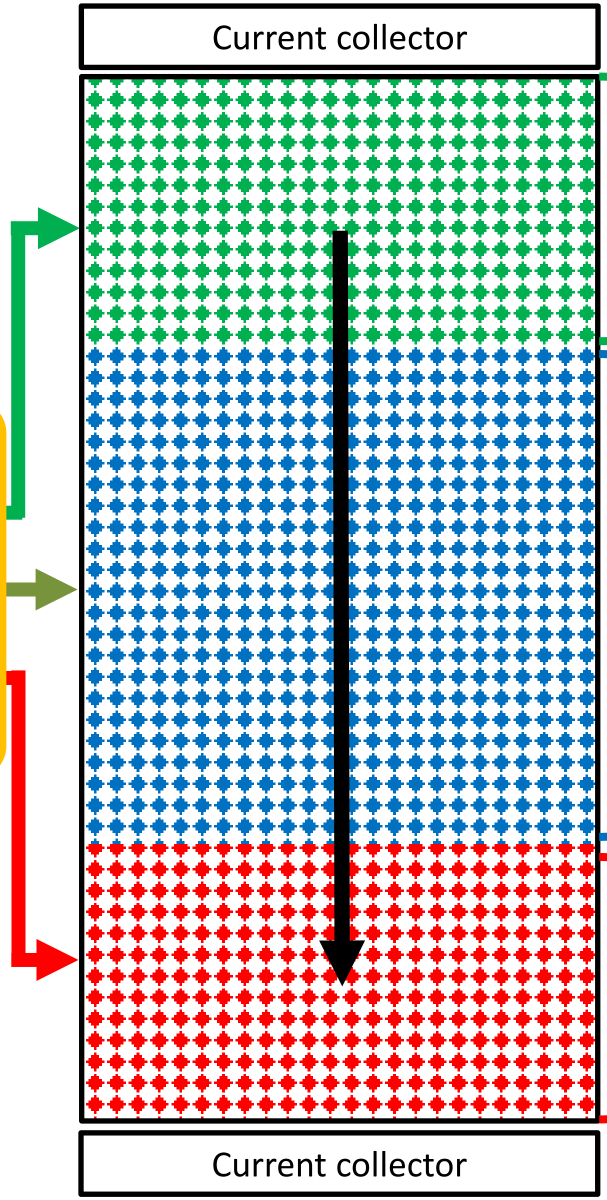
Suitable solid/spinel electrolyte composition: ionic conductivity versus stability

Enhanced micro-battery integration

Transparent interfaces *all-spinel* battery stack

matching crystal lattice





TiN, Pt, SiC, TiC, Cu

$Li_4Ti_5O_{12}$
TiO_2
a-Si

$LiAlO_2$
Li_4SiO_4
$Li_5AlSi_2O_3$
$LiMgTiO_3$
$LiTaO_3$
$Li_xMg_{1-2x}Al_{2+x}O_4$
$Li_{3x}La_{(2/3)}\square_{x(1/3)-2x}TiO_3$

$LiMn_2O_4$
MnO_2

TiN, Pt, SiC, TiC, Al

Suitable solid/spinel electrolyte composition: ionic conductivity versus stability

A suitable spinel electrolyte will be identified by **screening** of the composition with the aid of **combinatorial deposition in the PLD** system (4 targets)

The **interfaces** will be **optimized** for ionic transfer by compositional gradients and interfacial buffer layers

Fabrication of on-chip thin-film micro-batteries

PLD deposition technique. Three approaches:

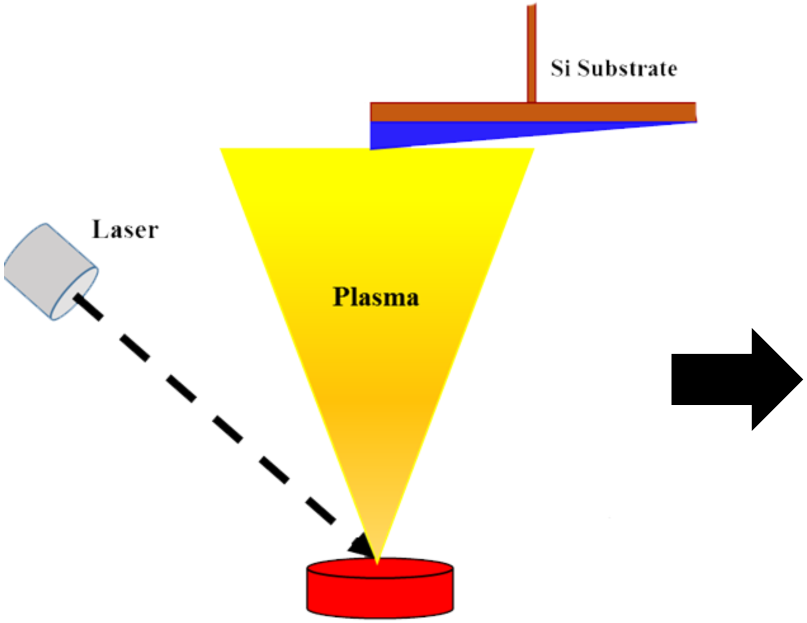
- Single layer
- Multilayer
- Combinatorial

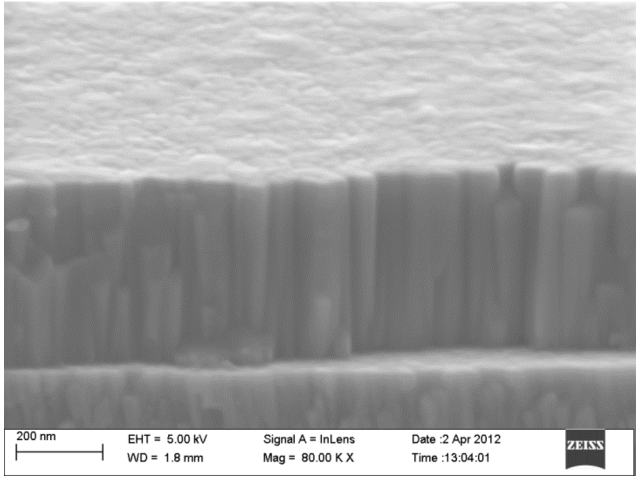
Optimization of thin film deposition

- Single target deposition:
  - TiO_2
  - Li_2O
  - MgO

- Stacking of single layers: formation of complex oxides

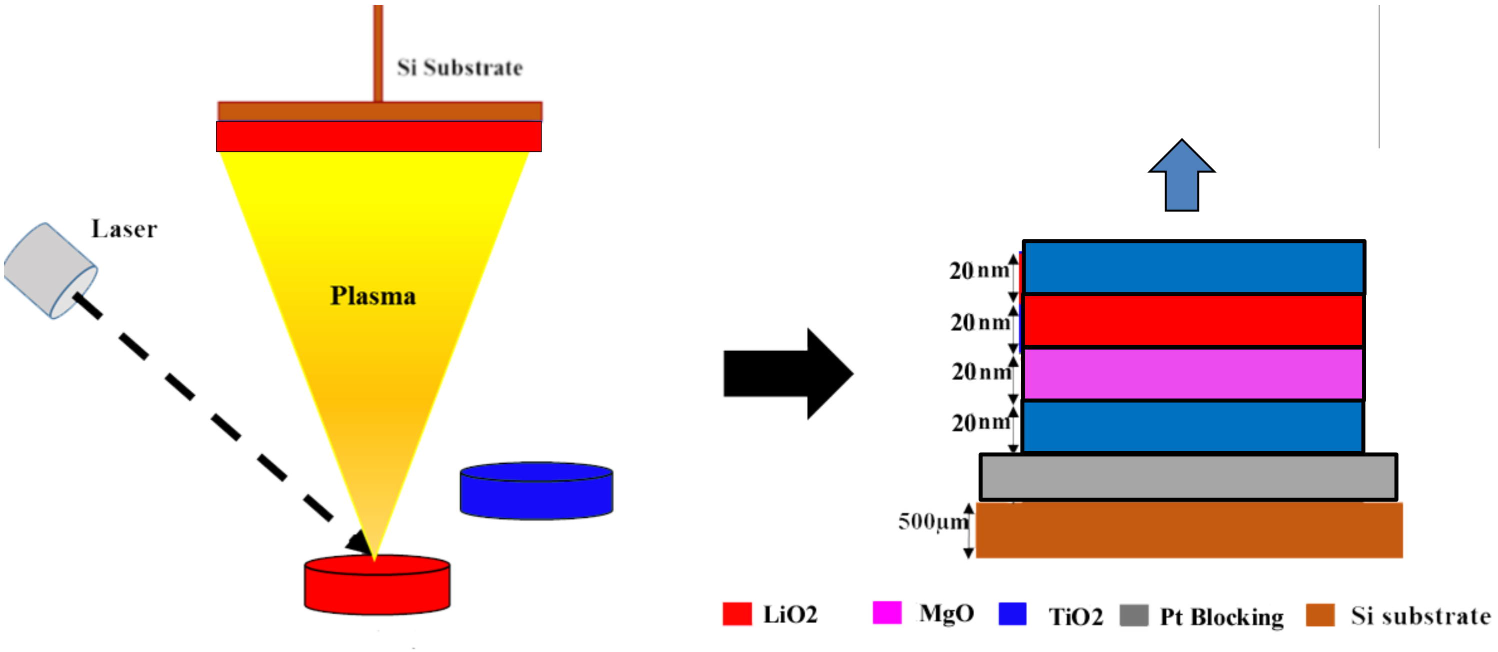
PLD deposition: single layer deposition





- Possibility of generating dense thin ceramic layers
- Good reproducibility of target stoichiometry
- Possibility of layer microstructure control (P, T, Laser energy…)

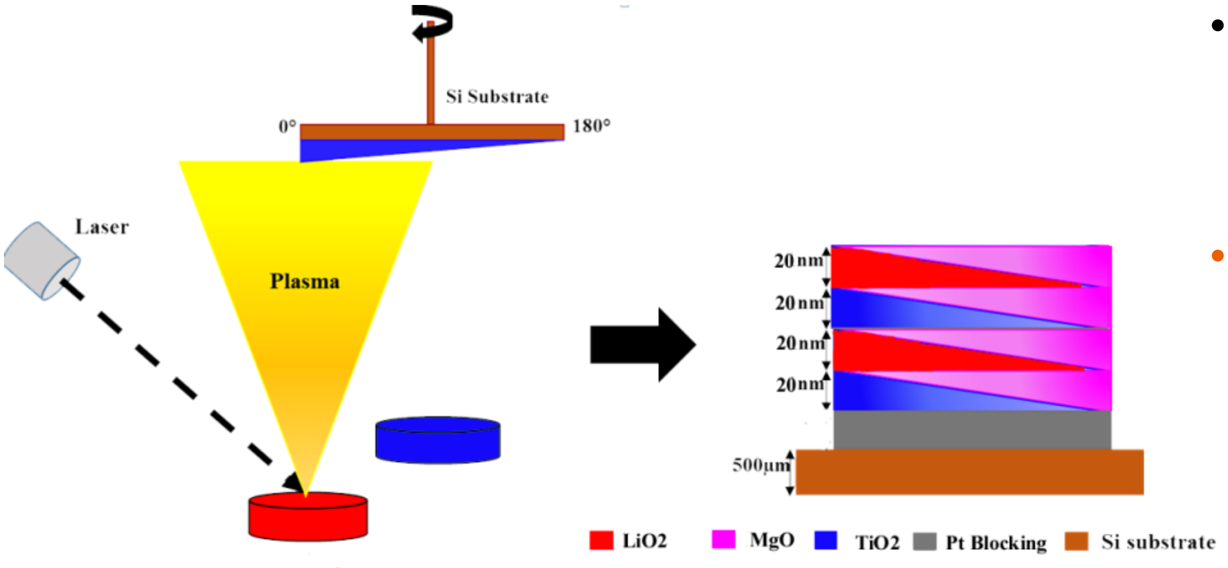
PLD deposition: Multi-layer deposition



Choosing right deposition parameters it is possible to:

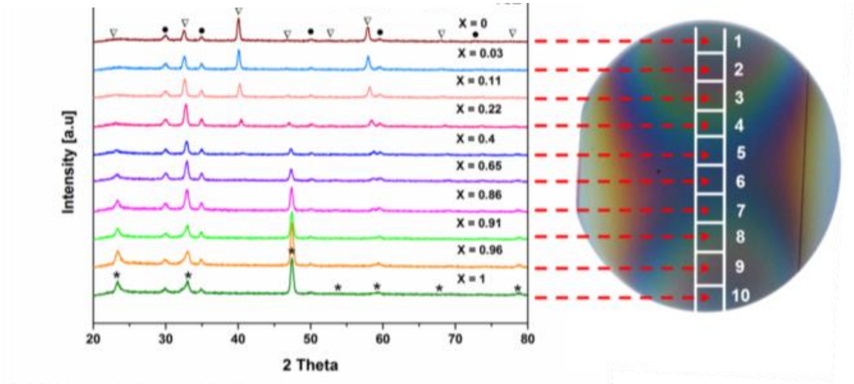
- Deposit multi-layers with good quality interfaces or
- Generate a complex material by thermal diffusion.

PLD deposition: combinatorial approach



- Large area system allows producing a combinatorial sample

- A full mapping of material composition can be generated in one shot



Summary & Outlook

Summary

- All-silicon harvester found feasible
- Delivered power expected to fulfill diverse WSN specs
- Solutions are cost-effective and do not require non-standard-IC processing

The Team

Luis Fonseca (CSIC, Project leader)
CSIC: Carlos Calaza, Marc Salleras, Jaume Esteve, Gonzalo Murillo, Carlos Camargo
Confindustria: Danilo Mascolo, Annamaria Raimondi, L. Rossi
Electrolux: Claudio Cenedese
IREC: Albert Tarancon, Alex Morata, M. Torrell, G. Gadea, J.D. Santos, M. Fehse
IMEC (Belgium): Philippe Vereecken, Cedric Huyghebaert, Brecht Put, Maarten Mees, Alfonso Sepulveda Marquez
IMEC (Netherlands): Rob Van Schaijkl, Martijn Goedbloed
STE: Paolo Moiraghi, Mauro Cortese
U. of Milano Bicocca: Dario Narducci, Laura Zulian
IMM-CNR: Alberto Roncaglia, Fulvio Mancarella

sinergy-project.eu
Contact: luis.fonseca@imb-cnm.csic.es

This work was supported by FP7-NMP-2013-SMALL-7, SiNERGY (Silicon Friendly Materials and Device Solutions for Microenergy Applications), Contract n. 604169

sinergy-project.eu
Contact: luis.fonseca@imb-cnm.csic.es